RCA

Broadcast Equipment

TR-70 and TR-60

TV Tape Recorders

CAVEC

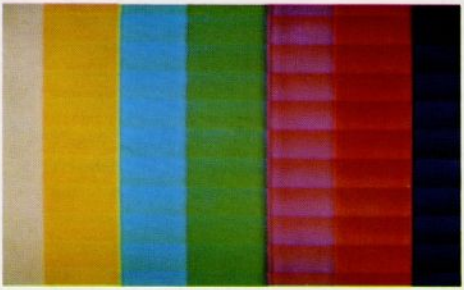
MI-35962A

MI-591631

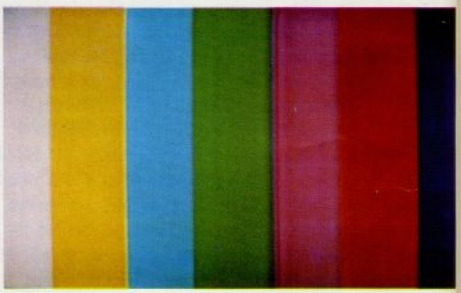
IB-32159

A. Color Bar Input Signal

B. Saturation Banding due to a 2 db loss in chroma on one channel caused by incorrect record current



C. Hue Banding due to playback with guide height misadjusted by 0.0007 inch



D. Errors shown in "B" and "C" eliminated by CAVEC (tape playback on TR-70 equipped with CAVEC and operating on highband)

Figure 1—Color Photographs Showing Tape Playback With or Without CAVEC (NTSC System)

TECHNICAL DATA TABLE

Operating Controls

a. VEC ON/OFF Switch:	Allows operator to bypass operation of VEC without affecting CAC
b. CAC ON/OFF Switch:	Allows operator to bypass CAC without affecting VEC
c. BURST RATIO Control:	Allows operator to adjust CAC to compensate for differences in the burst-to-chroma ratio of the recorded signal. Permits adjusting for normal chroma level for any recorded burst-to-chroma ratio in a range of ±6 db.

Chroma Amplitude Correction (on a Line-by-Line Basis)

a. *Operating Range:*	Corrects for deviations in chroma amplitude from normal of as much as ± 2db on high band recordings, or ± 3.5 dB on low band recording. (Not applicable to CCIR standards).
b. *Correction Factor:*	Reduces average chroma amplitude variations of 3 dB at blanking level by a factor of 24 dB for each line.
c. *Response Time:*	Corrects average chroma amplitude changes of 3 dB to within 0.5 dB of the final value not more than 0.1 second after these changes occur.

Chroma Phase Correction (on a Line-by-Line Basis)

a. *Operating Range:*	Corrects for chroma phase errors corresponding to 200 nanoseconds timing error.
b. *Correction Factor:*	Reduces average chroma phase variations for each line by a factor of 26 dB for line-to-line variations of 45 degrees or more. Reduces variations of 45 degrees or less to a maximum error of 3 degrees.
c. *Response Time:*	Corrects average changes of chroma phase to within 10 percent of final value no more than 0.1 second after these changes occur.

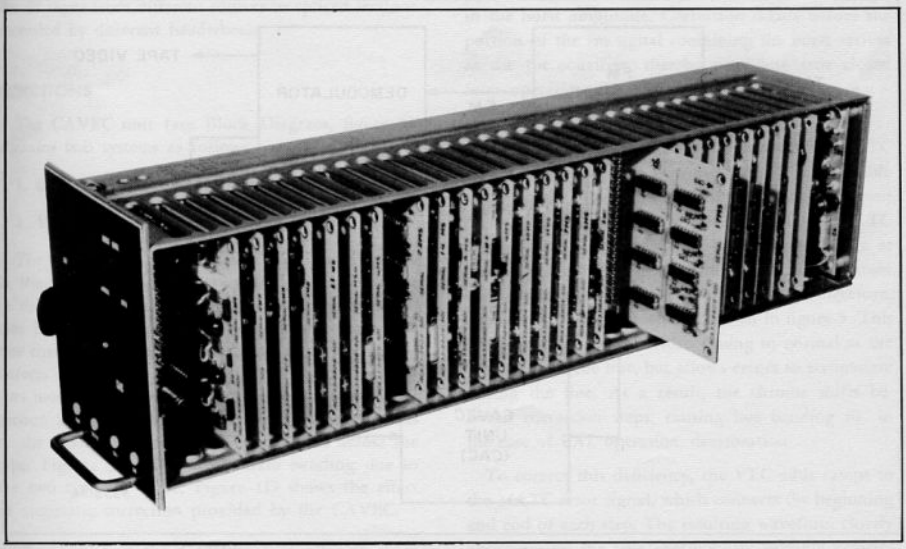


Figure 2—CAVEC Module

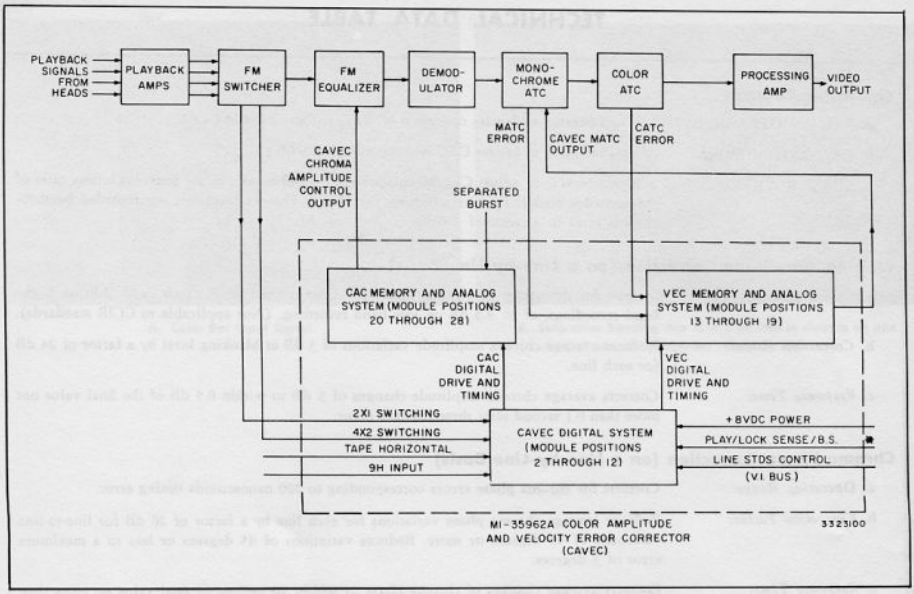


Figure 3—Simplified Block Diagram of CAVEC Unit in Tape Playback System

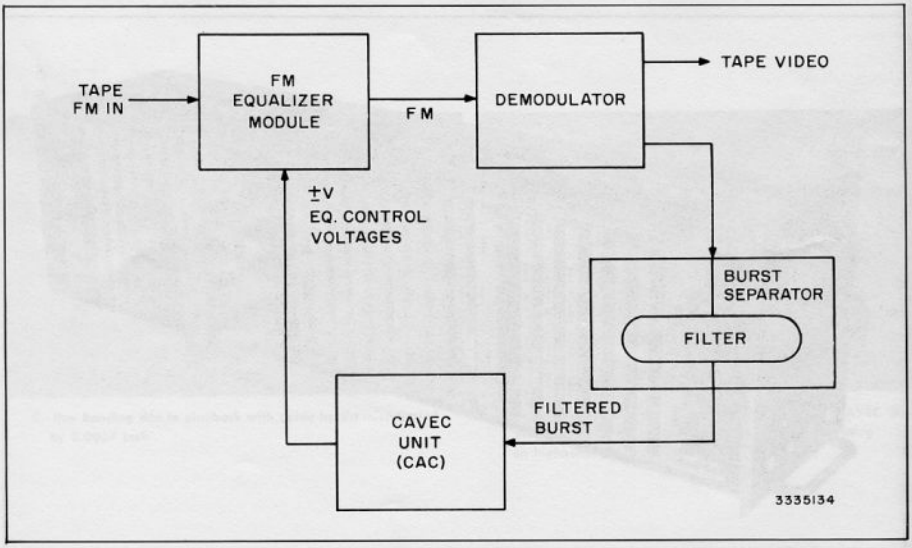


Figure 4—Simplified Block Diagram of CAC

GENERAL DESCRIPTION

The ES-43537 CAVEC (Chroma Amplitude and Velocity Error Corrector) accessory kit is designed for installation in RCA TR-70 TV Tape Recorders having serial number 7301 or higher, or TR-60 TV Tape Recorders having serial number 6001 or higher. ES-43537 contains the MI-35962A CAVEC module (see fig. 2) and the MI-591631 installation kit. Installation consists of adding two small circuit boards to existing modules in the machine and plugging the CAVEC module into a connector reserved for it on one of the module shelves (in location 626 for the TR-70 or Z3 for the TR-60). No harness installation is required since all interconnecting wires for the CAVEC module are already in the machine.

CAVEC improves color tape playback by automatically correcting, line-by-line, both amplitude and phase of the chroma component of the video output signal. This process permits making multiple generation tape copies of consistently high quality since it removes color errors originating in the master recording as well as those introduced by the playback machine. In addition, it eliminates the need for constant monitoring and readjustments normally required, especially when a program includes a number of tapes from different sources or spliced sections recorded by different headwheels.

FUNCTIONS

The CAVEC unit (see Block Diagram, figure 3) contains two systems as follows:

1. Chroma Amplitude Corrector (CAC).

2. Velocity Error Corrector (VEC).

The CAC corrects for frequency response variations in the video signal which produce saturation errors in the color picture. The VEC corrects for inaccuracies in head-to-tape velocity which cause undesired hue changes. Both errors are due to small mechanical defects inherent in quadruplex recording. These errors most often cause spurious colored bands in the picture 16 or 17 lines wide. Each band corresponds to the passage of one of the four heads across the tape. Figures 1B and 1C illustrate banding due to the two types of error. Figure 1D shows the effect of automatic correction provided by the CAVEC.

The circuits of the CAVEC are similar to those used in computers. Some are of the analog computer type, and others of the digital computer type. As shown in figure 3, the analog circuits are divided into two groups one for CAC and the other for VEC. The digital circuits are a single group shared by both VEC and CAC. The output signals which correct the errors are produced by the analog circuits. The digital circuits provide timing and control pulses to the analog circuits required for line-by-line correction.

The input to the CAC (see figure 4) consists of burst separated from the demodulated video. In the analog circuits the burst amplitude is compared to a reference level, and the resulting error voltage is stored in a capacity memory. The memory contains 64 capacitors, one for each line in the four head scans; thus, 64 errors are stored. At the beginning of each line the stored error voltage corresponding to the line is read out and converted into two push-pull voltages which constitute the CAC output signals. These signals are fed out of the CAVEC to an electrically controlled attenuator in the fm equalizer module. The attenuator automatically adjusts the fm equalization in a direction tending to reduce changes in the burst amplitude. Correction occurs before the portion of the fm signal containing the burst arrives at the fm equalizer, thereby providing true closed loop operation. Thus, the CAC resembles an automatic gain control system.

The VEC portion improves the monochrome ATC system of the machine by causing the MATC variable delay line to correct timing errors continously instead of in steps. In machines without CAVEC the MATC error signal is applied to the variable delay line at the beginning of each line and remains constant throughout the line. The error waveform therefore, appears as a series of steps as shown in figure 5. This type of signal restores video timing to normal at the beginning of the line, but allows errors to accumulate during the line. As a result, the chroma shifts between correction steps, causing hue banding or, in the case of PAL operation, desaturation.

To correct this deficiency, the VEC adds ramps to the MATC error signal, which connects the beginning and end of each step. The resulting waveform closely approximates the true continuously variable velocity error signal. To produce ramps of the correct slope,

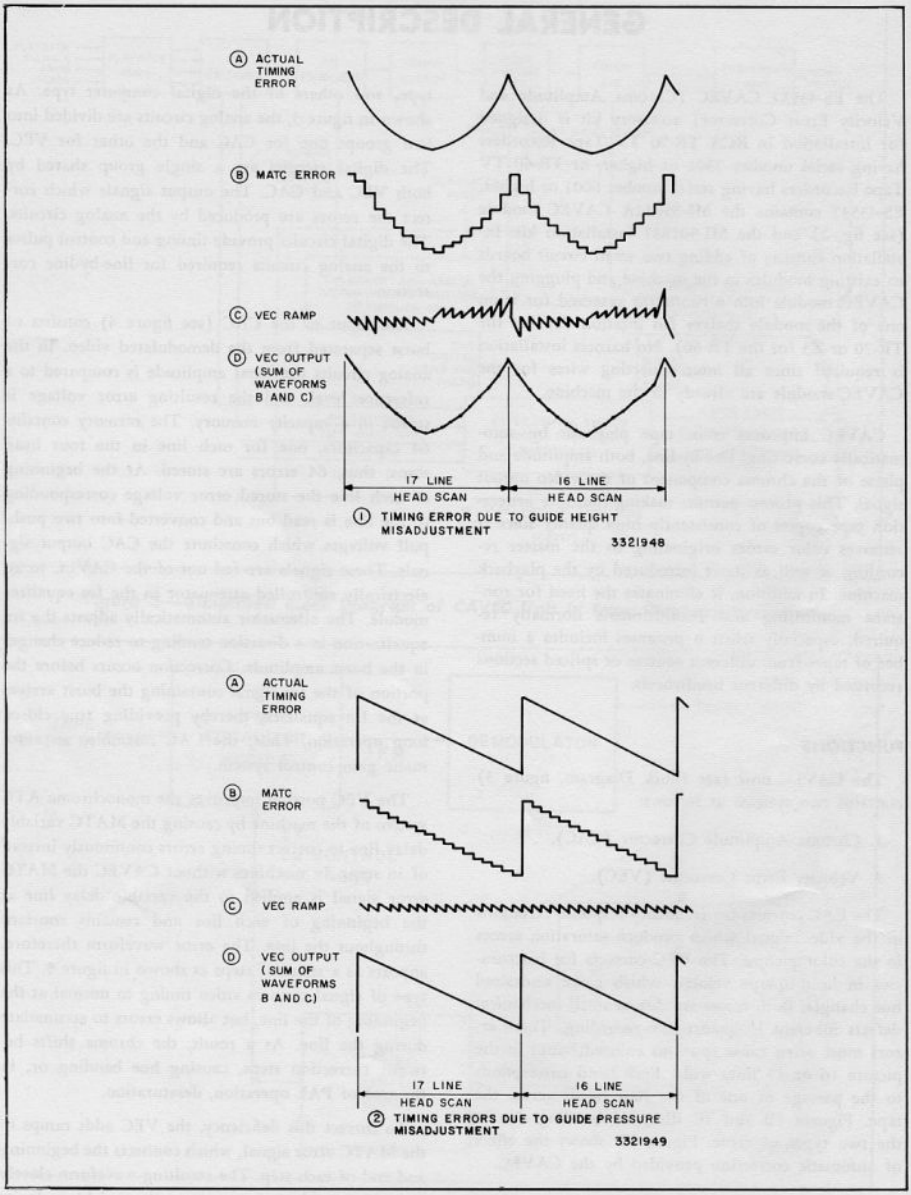


Figure 5—VEC Waveform Illustrations

the VEC analog circuits measure the differences between the successive step voltages and store the difference voltages in a capacitor memory similar to the one used by the CAC. The memory contains 64 capacitors, one for each of 16 lines in the four head scanning periods. (Since some head scan periods contain seventeen lines, the error stored in the sixteenth capacitor is used for both the sixteenth and seventeenth line). The time constant of the capacitor charging circuit causes the error voltage to stabilize after 24 headwheel revolutions. Each stored voltage, therefore, is an average for 24 revolutions. At the beginning of each line, the corresponding stored voltage is applied to a circuit which generates a ramp having a final height equal to the error. Each ramp is added to the corresponding MATC step, and the combined signal is fed out of the CAVEC to the circuits which control the MATC delay line.

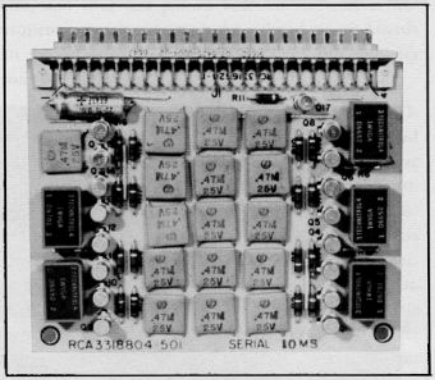


Figure 7—Typical Memory Board

CONSTRUCTION OF UNIT

Although the Cavec module, when mounted in the tape machine, looks like the other modules, its internal construction is entirely different (see fig. 2). Instead of one large circuit board, the Cavec unit contains a number of small printed circuit boards plugged, at right angles, into connectors on a wiring backplane which extends for the entire length of the assembly. The backplane has connectors, each containing 45 pins, for a maximum of 32 boards.

The digital system contains 11 boards, which occupy positions 2 through 12. Only five different types of digital boards are used. The principal components on these boards are integrated circuit packages of the dual in-line type. The packages contain logic circuits, such as gates and inverters, or timing circuits, such as one shots or flip-flops. All logic elements are of the diode-transistor logic (DTL) family.

Positions 15 through 18 are occupied by four identical boards which constitute the VEC memory. These boards contain storage capacitors, transformers, transistors, and semiconductor switches. A total of 64 storage capacitors is provided, 16 on each board. Each capacitor stores information pertaining to a particular line in a particular head scanning interval. (For example, line 1 of the head 1 interval.)

Positions 13, 14 and 19 contain the VEC analog boards. The components on these boards consist mostly of semiconductor switches and integrated cir-

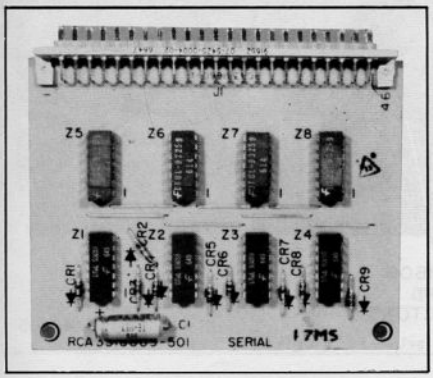


Figure 6—Typical Digital Board

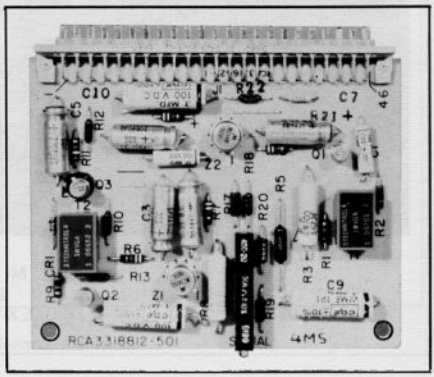


Figure 8—Typical Analog Board

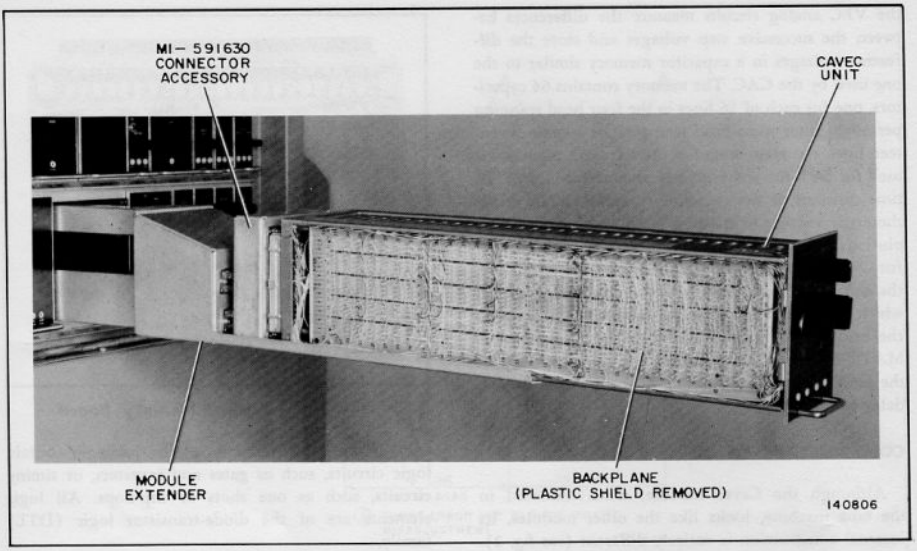


Figure 9—CAVEC Module Plugged Into Connector Accessory and Module Extender

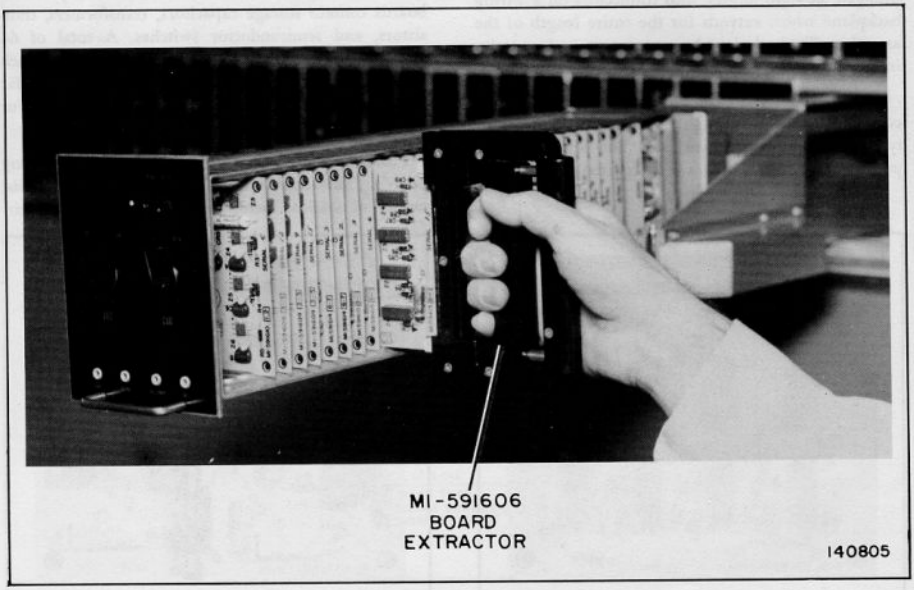


Figure 10—Use of Board Extractor

OPERATING PROCEDURES

SETUP ADJUSTMENTS

VELOCITY ERROR CORRECTOR

All timing adjustments have been made at the factory. Only the following adjustments on the VEC analog circuit boards are required:

1. Plug a standard module extender into the connector for the CAVEC module in the machine (location 626 for TR-70, or Z3 for TR-60). Insert the connector accessory (MI-591630) provided in the CAVEC installation kit into the module extender, and then plug the CAVEC module into the connector accessory. The backplane will now be accessible on the left, and the screwdriver potentiometers on the various circuit boards will be accessible on the right, without removing the boards from the module.

2. Place VEC switch on front panel in ON position.

3. Connect dc input of an oscilloscope to pin 33 of location 13 on the backplane of the CAVEC module. (This pin is available through a test point hole in the plastic shield.)

4. While playing back a locally recorded tape, adjust screwdriver potentiometer R15, of the circuit board in location 13 until dc voltage at pin 33 is 0 volts ± 0.5 volts.

5. With machine in STANDBY, observe signal at RAMP test point on the front panel of the module. Adjust R23 of the circuit board in location 14 until the ramps are flat (zero slope).

6. Calibrate the CRO monitor as follows:

a. Play back a locally recorded tape.

b. Press ATC ERROR button of CRO Switcher.

c. Place guide servo in MANUAL. Turn playback guide position control clockwise until height of any sloping line on the CRO is 80 I.R.E. units. This error signal amplitude corresponds to a timing error of 0.8 microsecond.

d. Press VEC button on CRO switcher and adjust R19 on the circuit board in location 19 until the average height of the VEC ramps on CRO is 50 I.R.E. units. (Note: The CRO is now calibrated so that 50 I.R.E. units, on VEC display corresponds to 50 nanoseconds.)

7. Connect oscilloscope to OUTPUT test point on CAVEC module. Adjust R6 of circuit board in location 19 until the ramps fill in the ATC staircase. (See figure 13.)

8. Observe VEC output on CRO. Turn guide position control counterclockwise until slopes of ramps reverse direction, and height of any one ramp is 50 I.R.E. units on CRO.

9. Reconnect oscilloscope to OUTPUT test point on CAVEC module and recheck adjustment of R6 on board in location 19 to make sure that ramps fill in staircase waveform.

CHROMA AMPLITUDE CORRECTOR

Attenuator Balance Adjustment

1. Place the FM equalizer module (523 in TR-70, X16 in TR-60) and the CAVEC module on module extenders. (If only one extender is available, use it for the FM equalizer.)

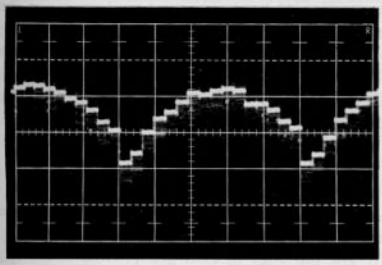
2. Place the equalizer potentiometer on the FM equalizer module in position 5.

3. Place the machine in the STOP mode. Press CRO CAC button and observe display on CRO.

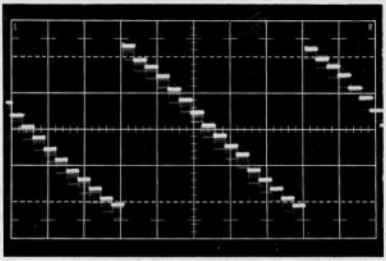
4. Adjust the attenuator balance control R19 on board number 24 of the CAVEC module (see fig. 103) until line is centered between two limit lines. (If CAVEC is not on extender it will be necessary to pull out CAVEC module, make trial adjustments of R19 and reinsert module until correct setting is obtained.)

Equalization and Burst Ratio

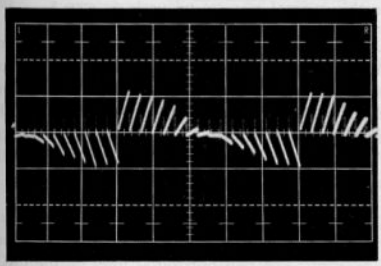
The following procedure may be performed with the machine operating in either high or low band standards. Once the adjustments are performed, on the selected band the CAC should perform properly on either band without repetition of the setup procedure.



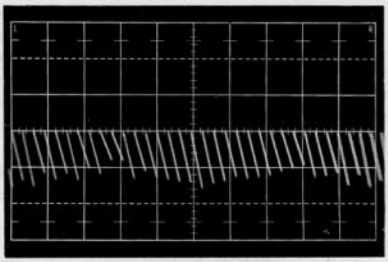
A. CAVEC "OUTPUT", TP-2, VEC Switch OFF; 0.4 μsec Scalloping Error (MATC ERROR 40 IRE Units). Sweep Rate 200 μsec/cm.



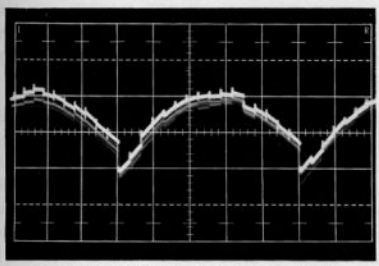
D. CAVEC "OUTPUT", TP-2, VEC Switch OFF; 0.8 μsec Penetration Error, (MATC ERROR 80 IRE Units). Sweep Rate 200 μsec/cm.



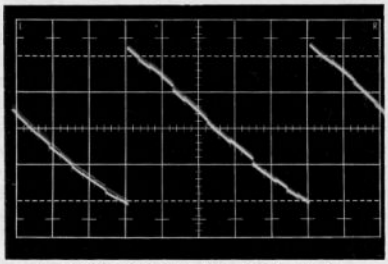
B. CAVEC "RAMP", TP-1, VEC Switch ON; Scalloping Error, Same as Waveform A; 0.2 v/cm, 200 μsec/cm.



E. CAVEC "RAMP", TP-1, VEC Switch ON; Penetration Error, Same as Waveform D; 0.2 v/cm, 200 μsec/cm.



C. CAVEC "OUTPUT", TP-2, VEC Switch ON; Scalloping Error, Same as Waveforms A and B; 0.2 v/cm, 200 μsec/cm.



F. CAVEC "OUTPUT", TP-2, VEC Switch ON; Penetration Error, Same as Waveforms D and E; 0.2 v/cm, 200 μsec/cm.

Figure 13—Typical VEC Waveform Photographs at Test Points

1. Feed a standard 75 percent color bar signal into the machine and make a test recording approximately five minutes long. The color bar input signal should have the specifications shown in figure 14, for 525 line operation, or in figure 15 for 625 line PAL operation.

2. Stop machine and place CAC switch on front panel of CAVEC in MANUAL or OFF position. On the FM Equalizer module place the step selection switch in position 5 and turn the equalization potentiometer to number 5 on the scale.

3. Press the CAC button on the CRO switcher and observe the CRO pattern. Two horizontal lines which represent the upper and lower limits of automatic equalization, will be visible. A third horizontal line, which represents the actual equalization voltage corresponding to the setting of the equalization potentiometer on module, may or may not be visible at this time, depending on the position of the potentiometer. Adjust the equalization potentiometer on 523 until this line is centered between the two limits. (See fig. 16B.) Do not adjust this control again throughout the procedure.

4. Make certain that the machine is set up properly for normal color playback on the correct standards, and then play the tape recorded in step 1.

5. Press DEMOD button on the CRO switcher, and set CRO sweep to horizontal rate. The color bar pattern on the CRO (fig. 16C) represents the superimposed outputs of the four playback channels, but the output of each individual channel can be identified by turning the equalization control on the corresponding playback amplifier module for channel 1, 2, 3, or 4 (modules 518 through 521 for TR-70 or X11 through X14 for TR-60) back and forth. The output of the selected channel will then appear to move up or down with respect to the other channel outputs. While observing the portion of the pattern corresponding to the green bar, identify the channel 1 signal by turning the equalization control for channel 1 (on module 518 or X11). Adjust this control so that the peak-to-peak amplitude of the channel 1 green bar signal is 82 IRE units for 525 line operation, or 88 IRE units for PAL.

6. Change the CRO sweep to the vertical rate and again observe the DEMOD pattern on the CRO. The video signals occurring within each of the 525 lines in a frame will now appear sequentially, from left to right (see fig. 16D). The group of 16 or 17 lines corresponding to head channel 1 will appear at the extreme left, followed by the groups corresponding to head channels 2, 3, and 4. This sequence will be repeated throughout the frame interval. Within each group the peaks of a given color bar will be at the same level for all the lines in the group, and therefore will form a horizontal line on the CRO, extending for the width of that section of the waveform. The peak levels for the same color bar, may however, differ in the four head channels, unless the equalization is the same for all channels (see fig. 16D). The top edge in each group, close to the 100 IRE unit level, corresponds to the positive peak of the yellow bar. Adjust the individual equalizer controls for channels 2, 3, and 4 (on modules 519, 520, 521, or X12, X13, X14) until the positive peaks of the yellow bar on these three channels are at the same level as on channel 1. Do not touch the channel 1 equalizer control (on module 518 or X11) since this control was set properly in step 5.

7. The second horizontal line from the bottom, in each head section, corresponds to the negative peaks of the blue bar. If these lines are not at the same level for all four channels, adjust the RESISTANCE controls on the channels 2, 3, 4 Playback Amplifier modules to minimize the differences in level. If necessary, repeat step 6.

8. Press the CAC button on the CRO switcher. Turn the CAC switch on the CAVEC module to the ON position. The two horizontal lines on the CRO display representing the limiting values of equalization voltage will again be present as during manual operation. Rotate the BURST RATIO control on the front panel of the CAVEC module, until a row of dots appears between the limit lines. (See fig. 16E.) These dots represent the individual equalization voltages for each line, required to maintain constant burst level. Adjust the BURST RATIO control to make the average level of the dots the same as the manual equalization level observed in step 3 (approximately halfway between the two limits).

9. Press the DEMOD button on the CRO switcher. While continuing to play back the color bars recorded in step 1, compare the CRO pattern obtained when the CAC switch on the CAVEC module is in manual with the pattern obtained when the switch is in AUTO. If the setup procedure has been followed correctly the chrominance amplitudes in AUTO should be the same as in MANUAL.

NOTE: The four screwdriver type potentiometers marked 1, 2, 3, 4 on the front panel of the CAVEC unit are not used in TR-70 or TR-60 machines.

Figu

Figure

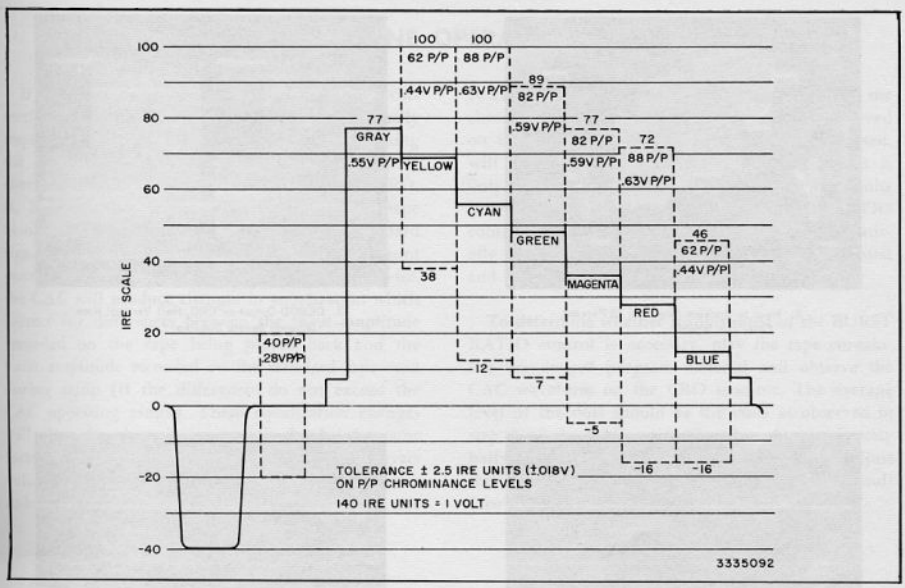


Figure 14—Waveform of Standard 75 Percent Color Bar Signal for 525 Line Operation

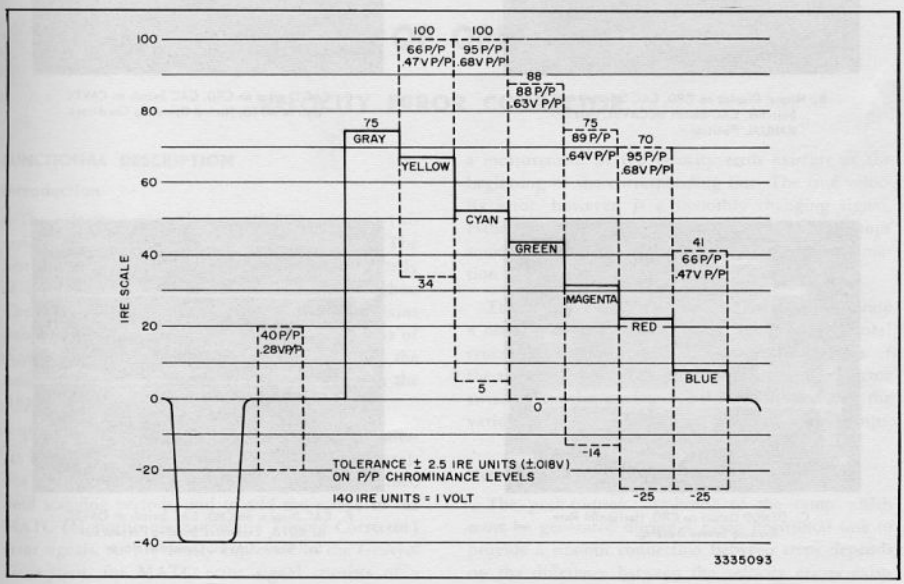
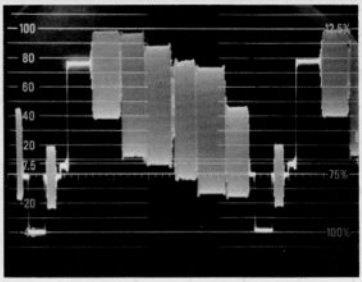
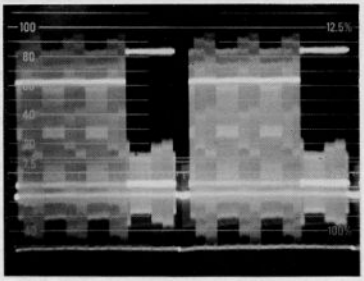


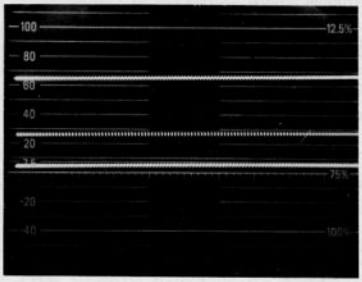
Figure 15—Waveform of Standard 75 Percent Color Bar Signal for 625 Line PAL Operation



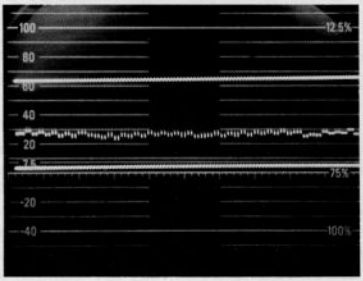
A. Input to Machine (Standard 75 Percent Color Bar Signal).



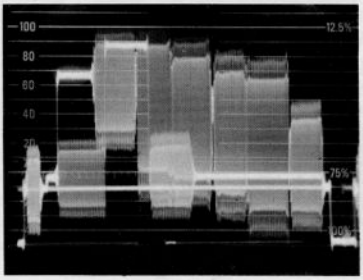
D. DEMOD Output on CRO, Half Vertical Rate, Showing Severe Banding.



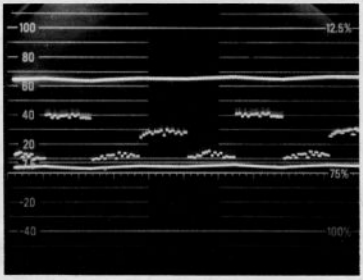
B. Normal Display on CRO, CAC Selected on CRO Switcher, CAC Switch on CAVEC Unit in MANUAL Position.



E. CAC Display on CRO, CAC Switch on CAVEC Unit in AUTO; Normal Operating Conditions.



C. DEMOD Output on CRO, Horizontal Rate, Showing Severe Banding.



F. CAC Display on CRO, CAC Switch on CAVEC in AUTO; Excessive Banding Present But Still Within CAVEC Correction Range.

Figure 16—Typical CAC Waveforms on CRO

ROUTINE OPERATION

If the setup procedures have been performed correctly no routine operating procedure is normally required for playing back most tapes, except turning the VEC and CAC switches ON and occasionally checking the VEC and CAC waveforms on the CRO. If, however, the chroma-to-burst ratios on the tape being played back differ from those of a standard signal, the BURST RATIO control on the front panel of the CAVEC must be readjusted. Otherwise, the CAC will produce changes in equalization which correct for differences between the burst amplitude recorded on the tape being played back and the burst amplitude recorded on the standard tape used during setup (if the differences do not exceed the CAC operating range). These equalization changes will alter the chrominance amplitudes by the same factor as the burst, thereby producing incorrect values of chrominance. (For example, if the chroma-to-burst ratios on the tape being played back are twice as large as on the standard recording, the chrominance amplitude of the green bar, observed on the CRO when the DEMOD button is pressed, will be correct (82 IRE units) when the burst is only half of its standard amplitude (20 IRE units instead of 40). (If, therefore, the BURST RATIO control is not readjusted, the CAC will automatically try to double the amplitudes of both the burst and chrominance signals.)

To determine whether readjustment of the BURST RATIO control is necessary, play the tape containing the desired program material and observe the CAC waveform on the CRO monitor. The average level of the dots should be the same as observed in step 8 of the CAC setup procedure (approximately halfway between the two limits). If necessary, adjust the BURST RATIO control to obtain this result (see fig. 16E).

THEORY OF OPERATION

VELOCITY ERROR CORRECTOR

FUNCTIONAL DESCRIPTION

Introduction

The velocity error corrector (VEC) contains two main groups of circuits, as shown in figure 17. The first group, called the analog system, consists mostly of operational amplifiers and semiconductor switches. The second group, called the digital system, contains pulse generators, counters, gates, and other forms of digital logic circuits. A brief introduction to the basic circuits used in the two systems is given in the *Appendix*.

The functions of the analog system are to generate a series of ramp signals (straight-line segments), one for each horizontal line in each of the four video head scanning periods, and to add the ramps to the MATC (Monochrome Automatic Timing Corrector) error signals. As previously explained in the *General Description*, the MATC error signal consists of a series of steps which change level at the beginning of each line. The amplitude of each step constitutes a measurement of the velocity error existing at the beginning of the corresponding line. The true velocity error, however, is a smoothly changing signal, rather than a series of steps. Addition of the ramps smooths out the steps to provide a better approximation to this signal.

The function of the digital system is to generate a number of timing pulses from the tape horizontal sync, 2 X 1 switcher and 4 X 2 switcher signals of the tape machine. These pulses control semiconductor switches in the analog system which perform the various functions required for generating the ramps.

VEC Analog System

The peak-to-peak amplitude of the ramp which must be generated during a given horizontal line to provide a smooth connection between steps depends on the difference between the velocity errors existing at the beginning and end of the line. The total velocity error must include the CATC (Color Auto-

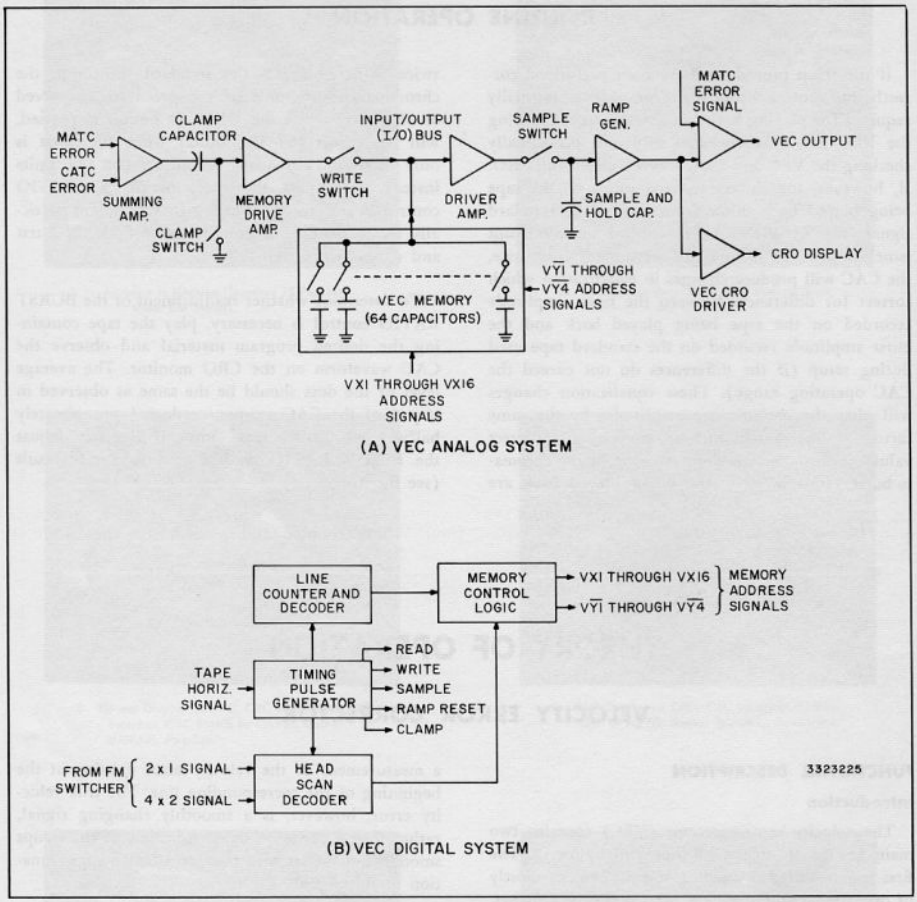


Figure 17—Simplified Block Diagrams of VEC

matic Timing Corrector) signal as well as the MATC signal. Consequently, the information required for generating the ramps is obtained by processing both the MATC and CATC error signals as shown in the block diagram figure 17. The two error signals for each line of a head scan are combined in a summing amplifier. This circuit amplifies each signal by a different amount, to obtain the required balance, and adds the results. For illustration purposes, the combined MATC and CATC signals for lines 10 through 13 are shown in the top line of the timing diagram, figure 18. Actually there are either 16 or 17 lines in a head scan on 525 line standards (15 or 16 lines on 625-line standards).

The line-to-line difference voltages required for determining the ramp heights are obtained by clamping the combined MATC and CATC error signal to ground for a short time, during each line. As shown in figure 18C, the clamping action places the level of each step at ground during the portion of the line remaining after clamping has taken place. The peak-to-peak amplitudes of the clamped waveform constitute the desired error differences.

As a typical example of clamp operation, consider the error differences for lines 10 and 11. The actual

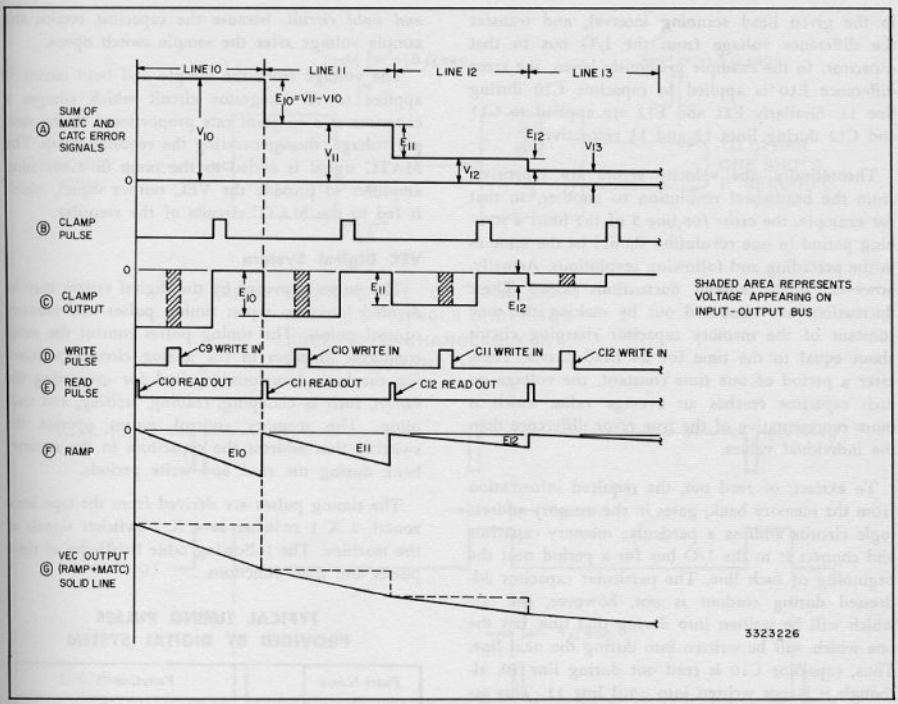


Figure 18—Simplified Overall Timing Diagram of VEC

amplitude of the combined error signal for line 10 is designated on the timing diagram as V10, and the amplitude for line 11, as V11. Throughout line 10, voltage V10 is applied from the summing amplifier to the input side of the clamp capacitor. When clamping occurs (during the clamp pulse shown in figure 18B) the clamp switch grounds the output side of the capacitor allowing it to charge to V10. When the clamp switch opens, the output side of the capacitor remains at ground for the remainder of line 10, since no discharge path exists. At the beginning of line 11, the voltage on the input side of the clamp capacitor jumps from V10 to V11, and, since the voltage across a capacitor cannot change instantaneously, the voltage on the output side must change by the same amount as the input side. (In effect, the change in voltage passes directly through the capacitor). The voltage on the output side of the capacitor, therefore, is the difference between V11 and V10, which is denoted by E10 on the diagram.

The clamped error signals are amplified and then fed to a semiconductor switch called the write switch. Once per line, for a short interval before the clamping operation a pulse from the digital system closes the write switch, thereby applying the signals to a bus (Input/Output or I/O bus) which goes to a bank of memory capacitors. As explained later, storage of the error signal differences in the memory bank provides information which allow prediction of the slope of each ramp at the beginning of the corresponding line.

The memory bank contains one capacitor for each possible line-to-line error difference in a complete rotation of the headwheel. Since a maximum of 17 lines can occur during the scanning period of each of the four video heads, resulting in a maximum of 16 error difference voltages per head scan, a total of 64 memory capacitors are provided in the bank.

While the write switch is closed, additional semiconductor switches in the memory circuits select (or address) a particular one of the 64 capacitors, which is associated with the given scanning line number

in the given head scanning interval, and transfer the difference voltage from the I/O bus to that capacitor. In the example previously given, the error difference E10 is applied to capacitor C10 during line 11. Similarly E11 and E12 are applied to C11 and C12 during lines 12 and 13 respectively.

Theoretically, the velocity errors are repetitive, from the headwheel revolution to another, so that for example, the error for line 5 of the head 4 scanning period in one revolution should be the same as in the preceding and following revolutions. Actually, however, small random fluctuations occur. These fluctuations are smoothed out by making the time constant of the memory capacitor charging circuit about equal to the time for 24 head passes. Thus, after a period of one time constant, the voltage on each capacitor reaches an average value which is more representative of the true error difference than the individual values.

To extract, or read out, the required information from the memory bank, gates in the memory address logic circuits address a particular memory capacitor and connect it to the I/O bus for a period near the beginning of each line. The particular capacitor addressed during readout is not, however, the one which will be written into during that line, but the one which will be written into during the next line. Thus, capacitor C10 is read out during line 10, although it is not written into until line 11. This action is required because generation of a ramp which will connect successive MATC steps requires advance knowledge of the slope.

For example, in order to obtain a smooth connection of the MATC steps for lines 10 and 11, the ramp must start at zero volts and end at $-E10$ volts. (See figure 18). Since the slope of this ramp is proportional to the height, or $-E10$, the value of E10 must be predicted at the start of the ramp, from the information available at that time. This information consists of the voltage previously stored in capacitor C10, since this capacitor will not be written into again until the next line.

During the read-out period, the voltage from the addressed memory capacitor is applied via the I/O bus to a driver amplifier (see figure 17). The driver output is connected to a semiconductor switch called the sample switch. For a portion of the readout time the sample switch closes and transfers the driver output voltage to a capacitor which serves as a short term or temporary memory. The sample switch and capacitor are referred to as the *sample and hold circuit,* because the capacitor retains the sample voltage after the sample switch opens.

The voltage from the sample and hold circuit is applied to an integrator circuit which charges a capacitor at a constant rate proportional to the sample voltage, thus generating the required ramp. The MATC signal is added to the ramp in a summing amplifier to provide the VEC output signal, which is fed to the MATC circuits of the recorder.

VEC Digital System

The pulses provided by the digital system may be divided into two types: timing pulses and memory control pulses. The timing pulses control the semiconductor switches in the analog circuits performing the basic functions required for generating the ramps, such as clamping, reading, writing, and sampling. The memory control pulses operate the switches that address the capacitors in the memory bank during the read and write periods.

The timing pulses are derived from the tape horizontal, 2 X 1 switcher or 4 X 2 switcher signals of the machine. The following table lists some of these pulses and their functions

TYPICAL TIMING PULSES PROVIDED BY DIGITAL SYSTEM

Pulse Name	*Function*
READ	Establishes time period, in each horizontal line, when memory capacitors are read out.
WRITE	Establishes time period, in each horizontal line, when memory capacitors are written into, or updated.
SAMPLE	Determines time period within the read interval when memory capacitor voltage on I/O bus is actually transferred to sample and hold circuit.
RAMP RESET	Resets ramp generator to allow generation of new ramp.
CLAMP	Determines time period when combined MATC and CATC input signals are clamped to ground, to derive error difference signals.
CLOCK	Provides horizontal rate timing reference.

The memory control pulses consist of two types, called the X and the Y signals. For the VEC system, there are sixteen X signals (VX1 through VX16) and four Y signals ($\overline{VY1}$ through $\overline{VY4}$). One X signal is provided for each horizontal line in

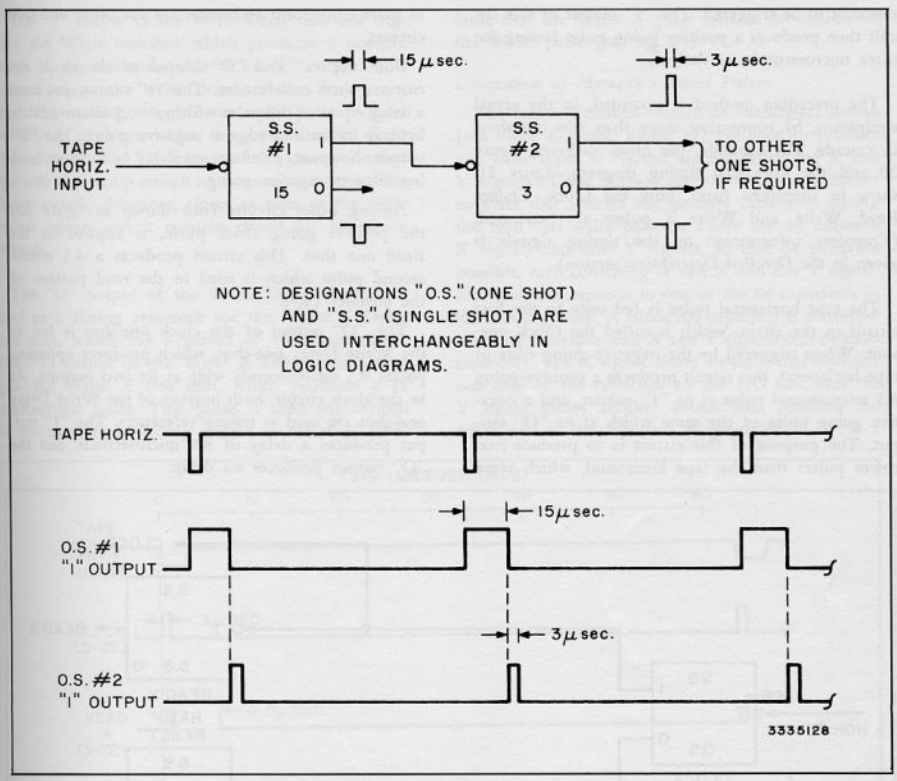


Figure 19—Use of One Shots in Cascade

a head scanning period and one Y signal is provided for each of the four head scanning periods. During the read and write periods of a given line, the corresponding X signal causes one side of four capacitors to be connected to the I/O bus, but the Y signal grounds the opposite side of only one of these capacitors, thereby completing its charge path. Thus, selection of each of the 64 capacitors in the memory is uniquely determined by the combination of one X signal with one Y signal.

Generation of Timing Signals

Since the various timing pulses are all referenced to the tape horizontal signal, the basic method of generating these pulses is by connecting two one-shot circuits in cascade. The first determines the delay of the output pulse with respect to tape horizontal, and the second, the width of the output pulse. For example, assume that it is desired to generate a pulse 3 microseconds wide, delayed by 15 microseconds from the leading edge of tape horizontal. To accomplish this, the tape horizontal pulse is fed to a one-shot having a period of 15 microseconds, and the output of this circuit is fed to another one-shot having a period of 3 microseconds (see figure 19).

As explained in the appendix, the "1" output of a one-shot is normally at the lower of its two possible levels, jumps to the higher level when the circuit is triggered, and returns to the lower level at the end of the pulse period. Each of the one-shots illustrated in figure 19, can be triggered only by a negative going transition. Consequently, at the negative-going (leading) edge of each horizontal pulse, the first one-shot is triggered and its "1" output produces a positive going pulse. At the end of the 15 microsecond pulse period of this circuit, the "1" output falls to the low level, causing the second

one-shot to be triggered. The "1" output of this circuit then produces a positive going pulse lasting for three microseconds, as desired.

The preceding method is extended, in the actual equipment, by connecting more than two one-shots in cascade. For example, the block diagram, figure 20 and the associated timing diagram, figure 21, show in simplified form, how the Clock, Clamp, Read, Write, and Write X pulses are generated. (Complete information on the timing signals is given in the *Detailed Description* section).

The tape horizontal pulse is fed only to the first circuit in the chain, which is called the Clock one-shot. When triggered by the negative going edge of tape horizontal, this circuit produces a positive-going 0.5 microsecond pulse at its "1" output, and a negative going pulse of the same width at its "O" output. The purpose of this circuit is to produce narrower pulses than the tape horizontal, which serve as more convenient references for the other one-shot circuits.

Both the "1" and "O" output of the clock circuit are used as reference. The "1" output produces a delay equal to the pulse width, or 0.5 microseconds, because its trailing edge is negative going. The "O" output, however, produces no delay because its leading edge is negative going.

Among other circuits (not shown in figure 20) the positive going clock pulse, is applied to the Read one shot. This circuit produces a 4.3 microsecond pulse which is used in the read portion of the memory cycle.

The "O" output of the clock one-shot is fed to the Write Delay one-shot, which produces opposing pulses 8.5 microseconds wide at its two outputs. As in the clock circuit, both outputs of the Write Delay one-shot are used as timing references. The "1" output produces a delay of 8.5 microseconds, but the "O" output produces no delay.

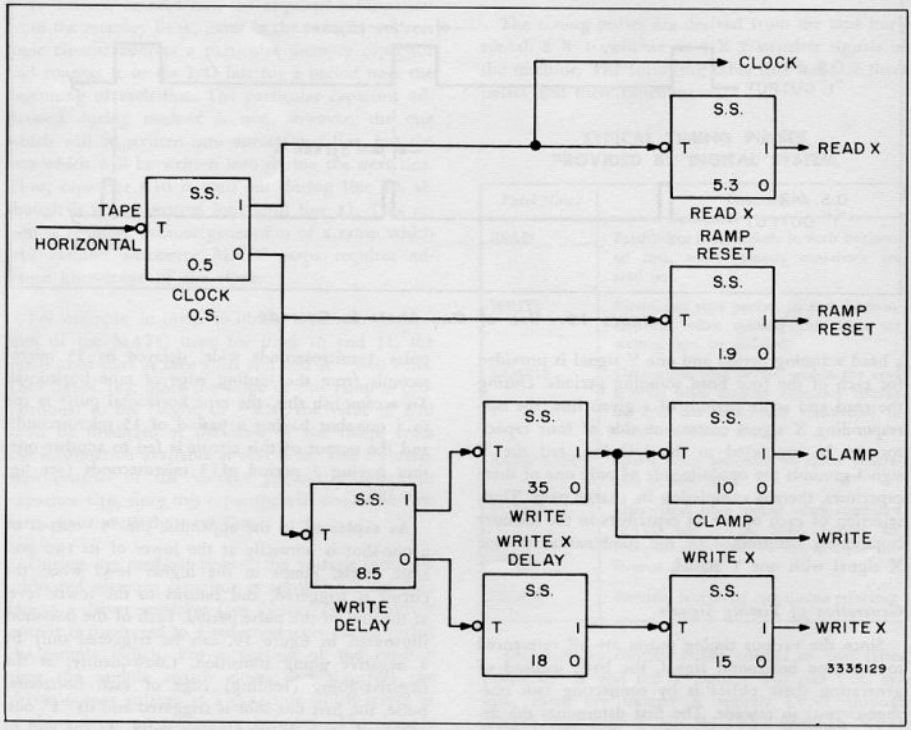


Figure 20—Partial Block Diagram of VEC Timing Generator Circuits

The "1" output of the Write Delay one-shot triggers the Write one-shot which produces a positive pulse 35 microseconds wide at its "1" output. This pulse operates the write switch of the analog system. The trailing edge of the write pulse triggers the Clamp one-shot, which has a pulse width of 10 microseconds. The "1" output of the clamp one-shot operates the clamp switch of the analog system. The clamp switch, therefore, closes as soon as the write switch opens, and it remains closed for 10 microseconds.

The "O" output of the Write Delay one-shot is used as a timing reference for the Write X Delay one shot, which has a period of 18 microseconds. The "1" output of the Write X Delay circuit triggers the Write X one shot, which produces a 15 microsecond pulse. This pulse is used for control of the memory switching matrix as described later. Note that the Write X pulse falls in the middle of the Write pulse (see fig. 21).

Generation of Memory Control Pulses

The memory control circuits of the digital system (see block diagram, figure 22) are used to produce two basic types of control signals called the X and Y signals. These signals control the semiconductor switches that address the memory capacitors during the read and write periods. There are 16 different X signals and four Y signals, so that 64 pairs are possible, each consisting of one X and one Y signal. Each pair corresponds to one of the 64 capacitors in the memory bank. A particular capacitor is addressed when its corresponding X and Y signals occur simultaneously. The X signal closes a switch that connects one side of the capacitor to the I/O bus, and the Y signal closes another switch that connects the other side of the capacitor to ground.

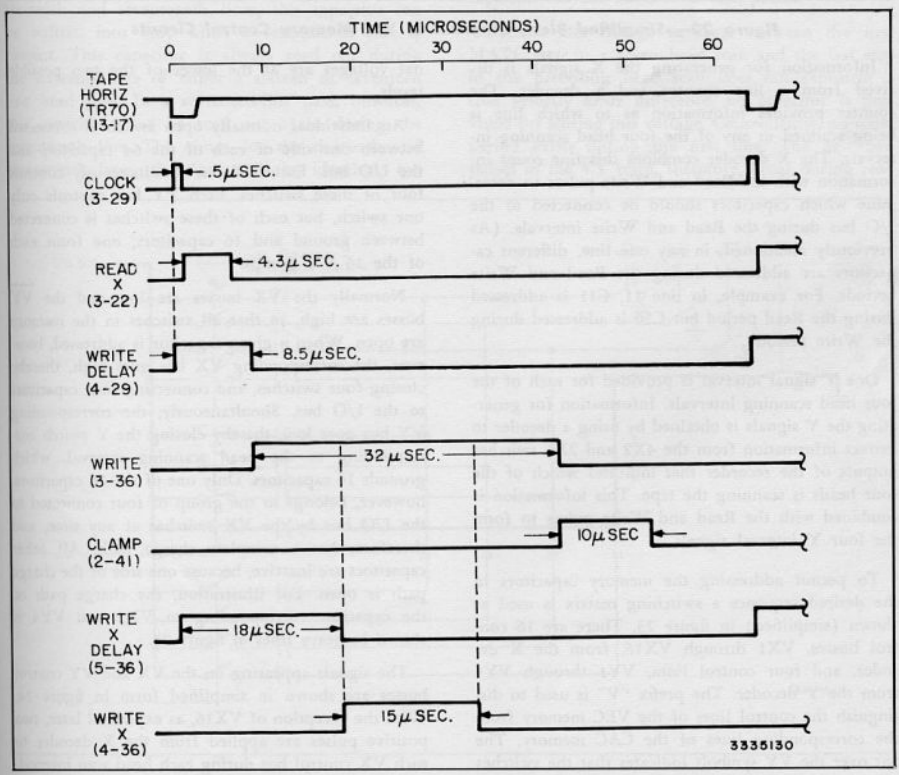


Figure 21—Simplified Timing Diagram of Horizontal Rate Timing Pulses

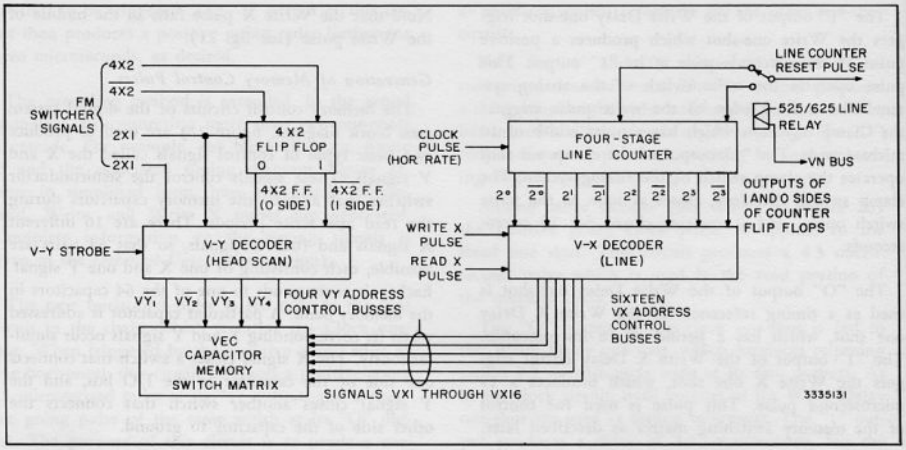


Figure 22—Simplified Block Diagram of VEC Memory Control Circuits

Information for generating the X signals is derived from a line counter and a decoder. The counter provides information as to which line is being scanned in any of the four head scanning intervals. The X decoder combines this line count information with the Read and Write pulses to determine which capacitors should be connected to the I/O bus during the Read and Write intervals. (As previously mentioned, in any one line, different capacitors are addressed during the Read and Write periods. For example, in line 11, C11 is addressed during the Read period but C10 is addressed during the Write period).

One Y signal interval is provided for each of the four head scanning intervals. Information for generating the Y signals is obtained by using a decoder to extract information from the 4X2 and 2X1 switcher outputs of the recorder that indicates which of the four heads is scanning the tape. This information is combined with the Read and Write pulses to form the four Y interval signals.

To permit addressing the memory capacitors in the desired sequence a switching matrix is used as shown (simplified) in figure 23. There are 16 control busses, VX1 through VX16, from the X decoder, and four control lines, VY1 through VY4 from the Y decoder. The prefix "V" is used to distinguish the control lines of the VEC memory from the corresponding lines of the CAC memory. The bar over the VY symbols indicates that the switches controlled by these busses are closed when the signal voltages are at the lower of the two possible levels.

An individual normally open switch is connected between one side of each of the 64 capacitors and the I/O bus. Each VX bus simultaneously controls four of these switches. Each VY bus controls only one switch, but each of these switches is connected between ground and 16 capacitors, one from each of the 16 VX groups.

Normally the VX busses are low and the $\overline{VY}$ busses are high, so that all switches in the memory are open. When a given capacitor is addressed, however, the corresponding VX bus goes high, thereby closing four switches, and connecting four capacitors to the I/O bus. Simultaneously, the corresponding VY bus goes low, thereby closing the Y switch corresponding to the head scanning interval, which grounds 16 capacitors. Only one of the 16 capacitors, however, belongs to the group of four connected to the I/O bus by the VX switches at any time, and therefore, has a complete charge path. All other capacitors are inactive, because one side of the charge path is open. For illustration, the charge path of the capacitor corresponding to VX2 and VY4 is shown in heavy lines in figure 23.

The signals appearing on the VX and VY control busses are shown in simplified form in figure 24. With the exception of VX16, as explained later, two positive pulses are applied from the X decoder to each VX control bus during each head scan interval. The first pulse connects the addressed capacitor to

the I/O bus during the read time of the particular scanning line, and the second pulse connects the same capacitor to the I/O bus during the write time of the next scanning line. This is done to permit predicting the slope of the ramp required for connecting the two MATC steps. (See fig. 18.)

The pulses on the VX1 through VX15 busses form an overlapping or interlaced sequence as shown in figure 24. For example, the first pulse VX pulse to occur during line 2 of a head scan period is VX2 and occurs during the read time of line 2, and the second pulse generated is VX1 and occurs during the write time of line 2. The pulses applied to VX16, however, do not conform to this pattern because, in succeeding headwheel revolutions, a seventeenth line occasionally occurs in each of the four head scan periods, although only 16 capacitors are provided for each head scan. Since the voltage stored in the sixteenth capacitor must serve for both the sixteenth and seventeenth lines, this capacitor can be written into only when a seventeenth line is present. This capacitor is always read out during the sixteenth line of either a sixteen or seventeen line head pass. In a seventeen-line pass, however, this capacitor must be read out again during the seventeenth line. The ramps for the sixteenth and seventeenth lines, therefore, will be identical, but little error will be introduced because the differences in slope between adjacent ramps are normally small.

During a 16-line head pass the only pulse appearing on the VX16 bus will occur during the read period of line 16. During a 17-line pass, however, three pulses will appear on VX16, the first during the read period of line 16, the second during the read period of line seventeen, and the third during the write period of line seventeen.

During the scanning period of each of the four video heads, a train of negative going pulses is applied from the Y decoder to the corresponding VY bus (see figure 24). Each of these negative going pulses corresponds to a positive going pulse on one of the sixteen VX busses. The corresponding VX and VY pulses occur at the same time, thereby closing both the X and Y switches of the addressed capacitor for the duration of the pulses.

Because the change in level between the first MATC step in a given head scan and the last step in the preceding head scan does not represent a true velocity error difference, no capacitor is provided for storing this voltage. Consequently, no write period exists during the first line. The first two pulses in the $\overline{VY}$ train, therefore, occur during read

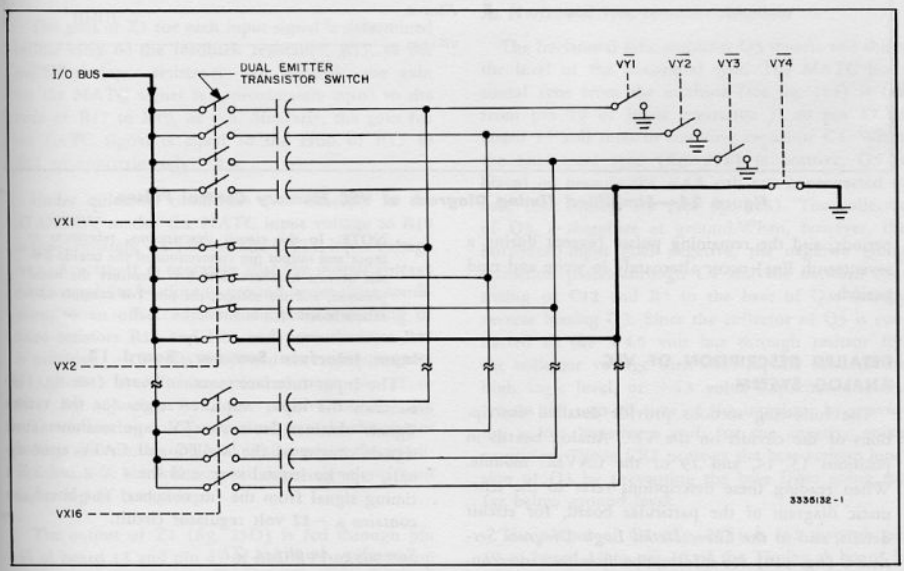


Figure 23—Simplified Schematic Diagram of VEC Memory Storage Matrix

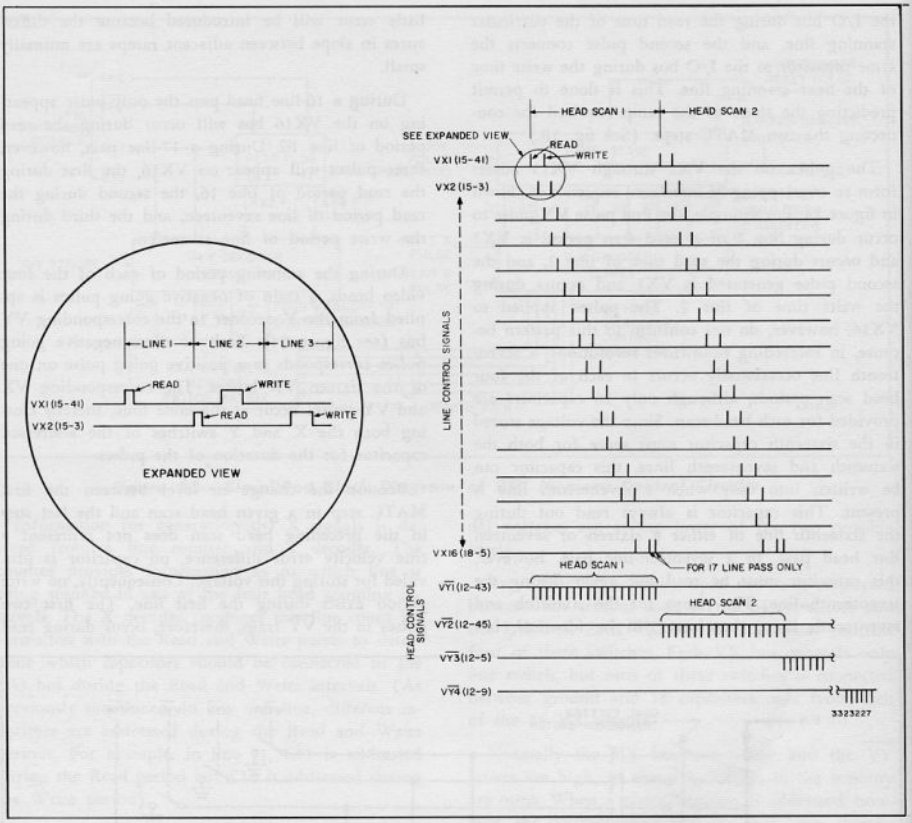


Figure 24—Simplified Timing Diagram of VEC Memory Control Pulses

periods, and the remaining pulses (except during a seventeenth line) occur alternately in write and read periods.

DETAILED DESCRIPTION OF VEC ANALOG SYSTEM

The following sections provide detailed descriptions of the circuits on the VEC Analog boards in positions 13, 14, and 19 of the CAVEC module. When reading these descriptions refer to the schematic diagram of the particular board, for circuit details, and to the *Cavec Detail Logic Diagram Section 6* (fig. 110) for information flow and interconnections. Occasional reference to the first section of the logic diagram, figure 105, will also be necessary.

NOTE: In the circuit descriptions, references to input and output pin connections of the boards consist of two numbers. The first identifies the board position, and the second, the pin. For example 13-5 means board 13, pin 5.

Input Interface Summer, Board 13

The input interface summer board (see fig. 123) contains the input amplifier stages for the various signals obtained from the TV tape machine. These signals consist of the MATC and CATC error signals, tape horizontal sync, and the 4 X 2 and 2 X 1 timing signal from the fm switcher. The board also contains a −12 volt regulator circuit.

Summing Amplifier, Z1

The function of the summing amplifier, Z1, is to amplify the MATC and CATC step signals and add

them to obtain an indication of the total velocity error in the tape video signal present at the start of each line.

The circuit of Z1 is similar to the summing amplifier described in the *Appendix*. The input signals (see waveforms, figure 25A, B, C) are applied through individual resistors to the inverting input of Z1. Feedback from the output terminal to the non-inverting input is provided by R17. The non-inverting input is grounded. Phase compensation to prevent oscillation is provided by capacitor C5. −12 volts dc is applied through R16 to pin 4 of Z1, and +12 volts dc is applied through R18 to pin 6. R16, C7, R18, and C6 filter the supply voltages.

The MATC signal from the machine is fed into the CAVEC module through pins 28 and 12 of the input/output connector J1 (see fig. 110). The signal (fig. 25A or 25B) is then fed through pin 23 of board 13 (13-23) to input resistor R10 of Z1. The CATC signal (fig. 25C) is fed into the CAVEC module through pins 25 and 9 of J1, and then routed through pins 15 and 31 of the Timing B board, to the input summer interface board. The timing B board is plugged into position 2, and the CATC signal from pin 31 of this connector is fed through pin 27 of board 13 (13-27) to input resistor R12 of Z1.

The gain of Z1 for each input signal is determined by the ratio of the feedback resistance, R17, to the individual input resistance. For example, the gain for the MATC signal is approximately equal to the ratio of R17 to R10, or −6. Similarly, the gain for the CATC signal is equal to the ratio of R17 to R12, or approximately −2.4.

Under quiescent conditions (for example in the STANDBY mode) the MATC input voltage to R10 is approximately +5.5 volts. The CATC input voltage is +1.5 volts. It is necessary that the output voltage of the amplifier be close to ground under these conditions, so an offset adjustment circuit consisting of fixed resistors R13 and R22 and potentiometer R15 is provided. −12 volts is applied through pin 15 to R13, and +12 volts is applied through pin 21 to R22. By adjusting R15, the positive or negative counterbalancing voltage required to make the output voltage zero can be obtained. This permits the amplifier to handle the full range of input signals without saturating or bottoming.

The output of Z1 (fig. 25D) is fed through pin 33 of board 13 and pin 43 of board 14 to the clamp circuit described under *Storage Driver,* Board 14.

−12 Volt Regulator

The −12 volt regulator circuit on board 13 consists of zener diode CR3, and regulator transistor Q4. The −20 volts from the machine is fed to the CAVEC module through pin 7 of the input connector J1 and then, through 13-45 to resistor R14. The base of Q4 is connected to the junction of R14 and the zener diode, CR3. R14 determines the base drive current and CR3 holds the base voltage constant at −13 volts.

The output voltage is fed through R16 to the negative supply terminal of summer amplifier Z1. This voltage is also fed out through pin 44 to a bus which goes to a number of circuits on the CAVEC module.

Interface Amplifiers

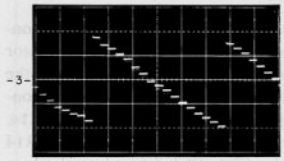
The interface amplifiers for the horizontal sync, vertical interval, 4 X 2 switcher and 2 X 1 switcher timing signals from the machine convert the voltage levels of these signals to the standard CAVEC logic levels of either 0 or +4.5 volts.

The input and output connections of these amplifiers are shown in the first section of the logic diagram, figure 105.

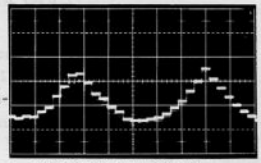
A. Horizontal Sync Interface Amplifier

The horizontal sync amplifier Q3 inverts and shifts the level of the horizontal sync. The MATC horizontal sync from the machine (see fig. 105) is fed from pin 19 of input connector J1 to pin 17 of board 13 and then to coupling capacitor C4. When the horizontal sync (fig. 25E) is positive, Q3 is biased on because the +4.5 volt bus is connected to base bias resistor R8 (see fig. 123). The collector of Q3, s therefore at ground.When, however, the horzontal input goes negative, the negative going transition passes through C4 and the network consisting of C12 and R7 to the base of Q3, thereby reverse biasing Q3. Since the collector of Q3 is connected to the +4.5 volt bus through resistor R9, the collector voltage then rises rapidly towards the high logic level, or +4.5 volts. Capacitor C12 decreases the turn-off time of the transistor by providing a low impedance path for the negative going transition. Diode CR2 protects the base-emitter junction of Q3 by preventing the base from going too far below ground level.

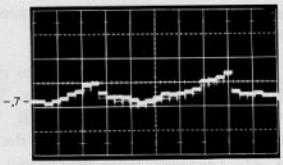
The output of Q3 (fig. 25F) is fed through pin 19 of board 13 to pin 10 of the Timing A board in position 3, where it is applied to another inverter,



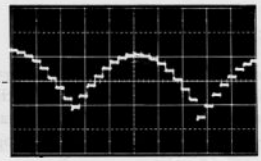
A. 13-23 (MATC IN), 0.2 v/cm
0.2 msec/cm
50 IRE units of error due to
tip penetration misadjustment



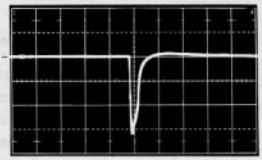
B. 13-23 (MATC IN), 0.2 v/cm
0.2 msec/cm
30 IRE units of error due to
guide height misadjustment



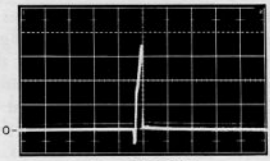
C. 13-27 (CATC IN), 0.1 v/cm
0.2 msec/cm



D. 13-33 (Z1 OUT), 1v/cm
0.2 msec/cm

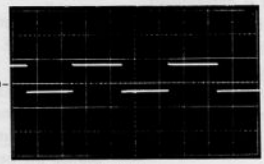


E. 13-27 (HOR SYNC IN)
2 v/cm, 2 msec/cm

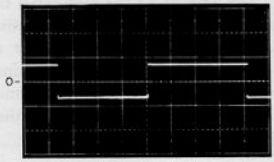


F. 13-19 (HOR SYNC OUT)
1 v/cm, 2 msec/cm

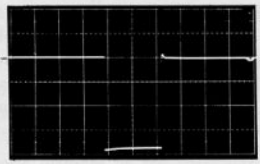
G. Top: 13-5 (2X1 IN), 1 v/cm
Bottom: 13-11 (4X2 IN), 10 v/cm
1 msec/cm



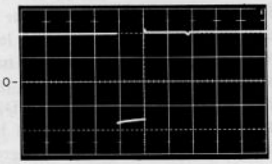
H. Q1 base, 1 v/cm
0.5 v/cm



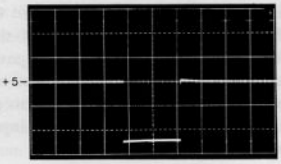
I. Q2 base, 1 v/cm
0.5 msec/cm



J. 13-9 (VERT-IN), 2 v/cm
100 usec/cm



K. Z2-1, 2 v/cm
0.2 msec/cm



L. 13-4 (VERT OUT) 2 v/cm
100 usec/cm

Figure 25—Waveforms, Board 13

and then to the clock one-shot. (See *VEC Digital System.*)

B. 4x2 Interface Amplifier

The 4x2 interface amplifier, Q2, inverts and shifts the level of the 4x2 switching waveform in a manner similar to Q3, previously described. The incoming 4x2 signal from the machine (fig. 25G) is fed from pin 18 of connector J1 through pin 11 of board 13 to input coupling capacitor C3. Q2 is normally biased on, and its collector therefore is at the low logic level, or ground. When, however, the 4x2 signal goes negative, Q2 becomes cut off and its collector rises to the high logic level or +4.5 volts. The output of Q2 is fed through 13-13 to 5-8 where it is applied to another inverter, and then to the 4x2 flip-flop circuit. (See description of VEC Digital System.)

C. 2x1 Interface Amplifier

The 2x1 interface amplifier, Q1, inverts and shifts the level of the 2x1 switcher signal in a manner similar to Q2 and Q3 previously described. The 2x1 signal from the machine (fig. 25G) is applied through pin 17 of connector, J1 to 13-5 and is then applied to the Q1 circuit through coupling capacitor C1. The output of Q1 is fed through 13-7 to a number of logic circuits as explained in the description of the *VEC Digital System.*

Vertical Interval Interface Amplifier

The Vertical Interval interface amplifier Z2, is an integrated circuit containing two inverters, Z2A and Z2B, which are connected in series. This circuit shifts the level of the vertical interval signal and decreases the rise and fall time, but provides no inversion.

The vertical signal from the machine (fig. 25J) is fed through pin 32 of connector J1 and 13-9 to coupling capacitor C8. The output of C8 is applied to a bias network consisting of R19 and R20, which is connected between the +4.5 volt bus and ground. When the vertical signal is positive, the bias voltage applied to the input of the first inverter stage Z2A, through pin 1 of Z2 (fig. 25K) is approximately +3.5 volts. The output of Z2A at Z2-6 is then at the low logic level, or ground. Since the input of Z2B at pin 9 is also low, the output of Z2B at Z2-8 is high or +4.5 volts. When the vertical input signal goes negative, the input to Z2A goes below ground, and the output of Z2A, rises to +4.5 volts. The output of Z2B, therefore falls to ground.

The output of Z2 (fig. 25L) is fed out through 13-4 to pin 38 of the Timing B board to a one-shot circuit having a pulse period of 830μ seconds. (See *VEC Digital System* description and fig. 105). This pulse is applied to a gate which prevents writing into the capacitor memory during the vertical interval.

VEC Storage Driver, Board 14

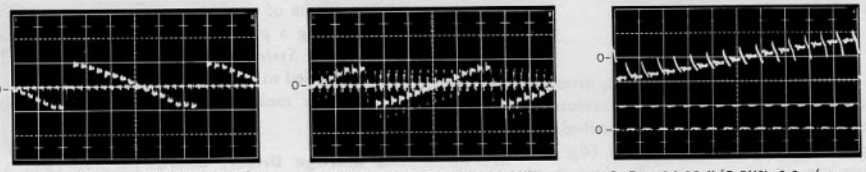
Board 14 contains the clamp error amplifier, and memory drive circuits of the VEC Analog system, shown in the upper section of the functional diagram, (figure 110). These circuits consist of clamp switch, Q1, memory drive amplifier, Z1, write switch driver, Q3, write switch, Q2 and memory read amplifier Z2.

Clamp Capacitor and Clamp Switch

The function of the clamp capacitor, C1, and switch, Q1, (see fig. 125) is to clamp the combined MATC and CATC error signal steps from the input summing amplifier on board 13, to ground during a portion of each horizontal line. The clamping process removes the dc level of the error signal, thereby providing an output voltage equal to the difference between successive step levels.

The error signal from the summing amplifier is applied through 13-33 and 14-43 to the input side of C1. The output side of C1 is connected to one emitter of the dual-emitter switch, Q1 and also to input resistor R3 of memory drive amplifier Z1. As explained in the *Appendix,* the dual-emitter switch is normally open, so that a very high impedance exists between its two emitters. When, however, a pulse of the correct polarity is applied to the primary of the drive transformer, T1, the switch conducts, effectively short-circuiting the two emitters.

The output of the clamp drive circuit on the board in position 4 is fed from 4-25 through 14-45 and resistor R2 to terminal 1 of the primary of T1. The clamp drive output level is normally low (zero volts), so that no difference of potential exists across the primary. During each line, however, (except line 1) the clamp drive output level goes high (+4.5 volts) for 10 microseconds starting approximately 40 microseconds after the tape horizontal signal. Q1 then conducts and effectively shorts the output side of C1 to ground for the duration of the clamp pulse, thereby allowing the capacitor to charge to the level of the error voltage step applied to its input side. When the clamp switch opens, the output side of C1 remains at ground, for the duration of the error step signal ap-



A. Junction C1 and R3 (Z1 IN), 0.5 v/cm
0.2 msec/cm
30 IRE units of error due to guide height misadjustment

B. Z1-5 (MEMORY DRIVE AMP OUT), 0.5 v/cm
2 msec/cm
30 IRE units of error due to guide height misadjustment

C. Top: 14-19 (I/O BUS), 0.5 v/cm
Bottom: 14-5 (WRITE PULSE), 2 v/cm
0.1 msec/cm

Figure 26—Waveforms, Board 14

plied to its input side, since the input side is held at the constant level of the step and no charge path exists. When, however, the step signal input changes to the next level, at the beginning of the next horizontal line, the change in level must pass through the capacitor to the output side, because the voltage across the capacitor must remain the same while the charge path is open. The voltage on the output side of the capacitor, therefore, jumps to a level equal to the difference between the step voltage of the line being scannel and that of the preceding line.

Memory Drive Amplifier, Z1

The clamped error signal differences from C1 are applied through resistor R3, to the inverting input, pin 2, of the memory drive amplifier Z1 (see fig. 125). This circuit is an operational amplifier of the differential input type described in the *Appendix*. The gain, which is determined by the ratio of the feedback resistance, R8, to the input resistance, R3, is approximately −0.8. Any dc offset voltage which may tend to accumulate because of imperfect clamping or amplifier drift is balanced out by a voltage applied from R5 to the non-inverting input, pin 1. This voltage is obtained from a divider consisting of fixed resistors R17, 18, 19, 20, and offset adjust potentiometer R23. Filtering of the negative 12 volt supply voltage to the amplifier is supplied by R7 and C4, and of the positive 12 volt supply by R6 and C3. Capacitor C2 provides phase compensation to prevent oscillation.

Write Switch Driver Q3, and Write Switch, Q2

The output of memory drive amplifier Z1 (fig. 26B) is fed to one emitter of the write switch, Q2. The other emitter of Q2 is connected through 14-19 to the I/O (Input/Output) bus of the capacitor memory bank.

The circuit of Q2 is similar to that of Q1, previously described, except that the input to the primary of the drive transformer, T2, is applied through a driver transistor Q3. The input to Q3 is obtained from the write inverter circuit on the board in position 4 (see fig. 105). The write inverter output is fed through 4-9 and 14-5 to the base current limiting resistor, R12, of Q3. The emitter of Q3 is connected through R11 to the +4.5 volt bus, but is clamped to a voltage slightly above ground by diode CR1. Normally the input signal level is low (ground) and consequently Q3 is cut off. Q2, therefore, is also cut off. Once in each line, however, starting 8.5 microseconds after horizontal sync the Write signal level goes high for 32 microseconds. Q3 conducts during this pulse period and its collector drives the write transformer T2.

During the write period, therefore, terminal 2 of the primary winding of T2 goes low, with respect to terminal 1 and the transformer is energized. As a result, Q2 conducts and connects the clamped error signal difference from the output of Z1 to the I/O bus. (See fig. 26C.)

Memory Read Amplifier, Z2

The purpose of the memory read amplifier, Z2, is to permit reading the memory capacitor voltages applied to the I/O bus during the read period of each line, without discharging the memory capacitors. Z2 is a voltage follower of the type described in the *Appendix*. This circuit merely provides isolation, since it has unity gain and does not invert the input

signal. Power supply filtering of the circuit is provided by R16 and C7 and R15 and C6. Phase compensation to prevent oscillation is provided by R22 and C10 and by C8.

The non-inverting input, pin 1, of Z1, is connected to the output emitter of Write switch Q2 which, as previously mentioned, is connected through 14-19, to the I/O bus. The output of Z2 is connected through R21, 14-37 and 19-43 to the Sample switch on the Sample and Hold circuit board, 19. The Sample switch closes only during a portion of the read period. Although the I/O bus is connected to the input of Z2 during the write period as well as the read period, the memory capacitor voltage is transferred to the sample and hold circuit only when the sample switch is closed.

Sample and Hold Board, 19

The Sample and Hold board contains the circuits shown in the lower blocks in section 6 of the logic diagrams, figure 110. These include the sample and hold circuit, Q1 and C1, ramp generator, Z1, ramp reset switch, Q2, output summing amplifier, Z2, and CRO amplifier Q3.

Sample and Hold Circuit

The Sample and Hold circuit consists of dual-emitter switch, Q1 and capacitor C1. One emitter of Q1 is connected through 14-43 to the output of the Memory Read amplifier, Z2, on board 14. The other emitter of Q1 (see schematic diagram, fig. 129) is connected to the junction of the hold capacitor, C1, and the input resistor (R2), of the ramp generator. Q1 is normally non-conducting. Once per line, however, for a period of two microseconds, a negative going pulse from the sample pulse inverter on the Timing B board (fig. 25A) is fed through 2-9 and 19-45 to the primary winding of the driver transistor T1 of the Sample switch, Q1. The switch then conducts, and feeds the memory read voltage to C1. The time constant of the charge circuits, determined by the resistance of R21, on board 14, and the capacitance of C1, is so short that C1 charges to the full memory read voltage in the 2 microsecond sample pulse period. C1, therefore, serves as a short-term or temporary memory. The Sample pulse occurs within the Read period of each line (1.9 microseconds after tape horizontal). The voltage applied to C1 is thus, the same as that on the storage capacitor connected to the I/O bus during the Read interval.

Ramp Generator, Z1, and Ramp Reset Switch Q2

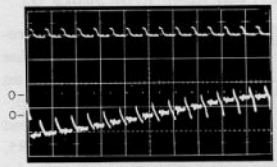
The function of the ramp generator, Z1, is to produce a ramp voltage during each horizontal line having a slope determined by the voltage then on the sample and hold capacitor C1. This circuit functions as described in the *Appendix*. R2 is the input resistor and C5 is the feedback capacitor. R4, C3, R5, C4, filter the power supply voltages. C2 provides phase compensation to prevent oscillation. R3 and C6 provide a small amount of current to the non-inverting input, pin 1 of Z1, required to bias the circuit.

The two emitters of the Ramp Reset switch, Q2 are connected across the feedback capacitor C2. A negative pulse from the Ramp Reset gate on board 3 (fig. 27C) is applied from 3-25, through 19-35 to the primary of drive transformer, T2 during the last 0.7 microseconds of each sample period. This pulse energizes Q2, thereby providing a direct short between the two emitters which completely discharges the feedback capacitor, C5. The reset switch is isolated from the sample and hold capacitor by R2.

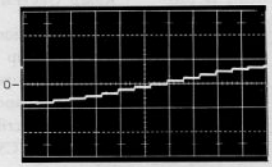
During the discharge period, the output voltage at pin 5 of Z1 drops to ground. At the end of the sample pulse Q2 opens and removes the short. A constant current determined by the input voltage from C1 then flows from the output terminal into C5, which charges C5 at a rate proportional to the current. The voltage across C5 also increases at a constant rate, thereby producing the required ramp voltage at the output of Z1. Since the input voltage (fig. 27B) is applied to the inverting input of Z1, pin 2, the ramp voltage (fig. 27C) charges in a direction opposite to the polarity of the input voltage. For example, if the voltage on the sample and hold capacitor, C1, is positive with respect to ground, the ramp voltage waveform will slope downward. Conversely if the input voltage is negative with respect to ground, the ramp will slope upward.

The ramp is fed from the output of Z1 to a voltage divider consisting of fixed resistors, R16 and R17, and potentiometer R6. From the arm of R6, the ramp is applied to the output summing amplifier Z2, where it is combined with the MATC signal. R6 permits adjusting the amplitude of the ramp to provide a smooth connection between MATC steps.

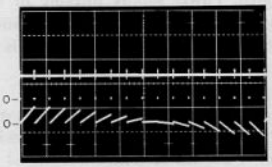
The ramp from the output of Z1 is also fed through R18 to the CRO amplifier, Q3, for monitoring. A potentiometer, R19, in the base circuit of Q3 permits adjusting the amplitude of the ramp output to calibrate the CRO display of VEC error.



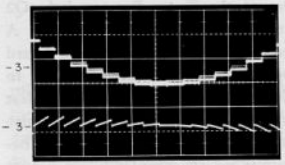
A. Top: 19-45 (VEC SAMPLE) 2 v/cm
Bottom: 19-43 (SAMPLE AND HOLD IN) 0.5 v/cm
0.1 msec/cm



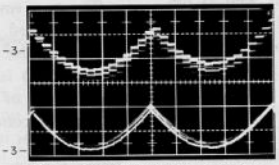
B. 19-37 (Z1 IN), 0.5 v/cm
0.1 msec/cm
30 IRE units of error due to guide height misadjustment



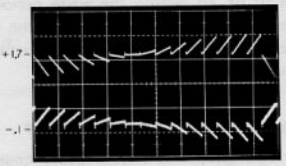
C. Top: 19-35 (RAMP RESET), 5 v/cm
Bottom: 19-33 (RAMP OUT), 0.5 v/cm
0.1 msec/cm
30 IRE units of error due to guide height misadjustment



D. Top: 19-17 (MATC IN), 0.2 v/cm
Bottom: 19-39 (RAMP IN), 0.2 v/cm
0.2 msec/cm



E. Top: 19-17 (MATC IN), 0.2 v/cm
Bottom: 19-11 (VEC OUTPUT), 0.2 v/cm
0.2 msec/cm



F. Top: Q3 Collector, 0.5 v/cm
Bottom: Q3 base, 0.2 v/cm
0.1 msec/cm

Figure 27—Waveforms, Board 19

Output Summing Amplifier, Z2

The Output Summing amplifier, Z2, is actually a balanced differential input amplifier (see *Appendix*). One of the input signals to Z2 is the ramp from the arm of potentiomteer R6, which is applied through R8, to the inverting input. The other signal is the MATC error voltage from the machine (fig. 27D) which is fed from pin 28 of connector J1 through 19-17 and R15 to the non-inverting input. The amplitude of the ramp input to Z2 increases as R6 is turned clockwise. The amplification of the ramp signal, determined by the ratio of feedback resistor R10, to input resistor R8, is approximately −1, while the gain of the MATC signal is approximately +1. The output voltage of Z2, therefore, is approximately equal to the MATC voltage minus the ramp voltage. As described, previously, the output of ramp generator Z1 is inverted with respect to the sample voltage. The effect of subtraction therefore is the same as if a ramp of the correct polarity were *added* to the MATC signal.

The combined ramp and MATC signal, is fed to a noise filter consisting of R23 and C20 and then through 19-11 (see fig. 27E) to test point TP2 (OUTPUT) on the CAVEC front panel and to terminal 29 of connector J1. The signal at J1-29, which constitutes the VEC output, is fed to the MATC circuits of the machine. (See block diagram, figure 110.)

CRO Amplifier, Q3

The ramp signal is fed from the output of Z1 through R18 to the CRO amplifier Q3. The output of Q3 (fig. 27F) is fed through C14 and 19-29 to test point TP1 (RAMP) on the CAVEC front panel, and also through J1-30, to the VEC pushbutton circuit of the CRO monitor switcher. Potentiometer R19, in the base circuit of Q3 permits adjusting the amplitude of the ramp for calibrating the VEC CRO display, (see *Operating Procedures*). The gain of the CRO amplifier is determined by the ratio of R20 to R22. Power supply filtering is provided by C13, C15 and R21.

VEC ON/OFF Switch

The VEC ON/OFF switch, S1, on the CAVEC front panel (see (fig. 110) is connected through 19-39 and C19 to the arm of potentiometer R6, in the ramp input to the summing amplifier Z2. When the switch is in the OFF position, it effectively shorts the ramp input to ground through C19. Since Z2 has unity gain for the MATC input signal, this signal then passes through Z2, without alteration, to the VEC output and back to the machine. The MATC system, therefore, performs as it did before installation of the CAVEC.

DETAILED DESCRIPTIONS OF VEC DIGITAL SYSTEM

The following sections provide detailed descriptions of the VEC digital logic and memory circuits. These circuits are on the boards listed in the following table.

VBC DIGITAL AND MEMORY BOARDS

Position in CAVEC Module	*Name of Board*	*Qty.*	*MI Number of Board*
2	Timing B	1	MI-591610-A
3, 4, 5	Timing A	3	MI-591609-A
6, 7	Control and Gating	2	MI-591614
8, 9, 10, 11	X Decoder	4	MI-591615
12	Y Switch Driver	1	MI-591612
15, 16, 17, 18	VEC Storage Board	4	MI 591607

Unlike the Analog boards, previously described, each digital board is a collection of similar types of circuits (for example, one shots, flip-flops, or gates) grouped together for convenience. The same types of digital boards are used in several different locations in the CAVEC module. Since, the digital circuits therefore cannot conveniently be traced directly on the individual schematic diagrams of the boards, these circuits are described with reference to the logic diagrams, figures 105 through 109.

The individual board schematic diagrams are, however, required for isolating troubles to specific components and parts replacement. Cross reference tables, therefore, are provided in the *Maintenance Procedures section* to permit identifying each element on the logic diagrams by schematic symbol number and function.

For simplification, the following abbreviated notation is used in the description of the digital system:

1. If the function controlled by a given timing signal is actually performed when the signal is at its low (relatively negative) level a bar is placed over the signal designation. Conversely, if the function is performed when the signal is at its high (relatively positive) level no bar is used. For example, the designation Sample indicates a signal that is low when sampling occurs, and the designation Clamp indicates a signal that is high when clamping occurs.

2. As in the analog description, input and output terminal numbers of the boards are indicated by two numbers. The first identifies the location of the board, and the second, the pin number. For example, 4-25 means pin 25 of the board in position 4.

The circuits are discribed in the same order as they appear on the logic diagrams, starting with section 1 (figure 105) and ending with section 5 (figure 109). Although the logic diagrams include the CAC digital circuits, only the VEC circuits and those common to both VEC and CAC are described in this section. For information on the CAC circuits see *Detailed Descriptions of CAC.*

NOTE: For an introduction to use of the logic symbols and operation of the basic logic circuits, refer to the *Appendix.*

Generation of Horizontal Rate Timing Signals

All of the basic timing pulses listed in the table on page 42 are produced by one-shots, gates, and inverters on the Timing B circuit board (position 2) and the three timing A boards (positions 3, 4, 5). The logic of these circuits is shown in the first section of the logic diagram, figure 105. For comparison, idealized waveforms of the pulses are shown on the VEC Detailed Timing Diagram, figure 28. The actual pulses are shown in the waveform photographs, figures 29 and 30. In general the actual waveforms depart from the ideal rectangular shape because the pulses are fed to reactive loads, such as transformers, in the analog circuits.

Horizontal Sync Processing

As previously described under *Analog System,* tape horizontal sync from the machine is fed through J1-19 and 13-7 to the horizontal sync interface amplifier on board 13. This circuit (see fig. 105) inverts the signal and changes its voltage swing to conform to the standard logic levels of 0 and +4.5 volts.

The output of this stage is fed through 13-19 and 3-10 to an inverter on board 3. The inverter output at 3-9 has the same polarity as the original sync pulse, but a shorter rise and fall time, because the inverter responds very rapidly to changes in input voltage.

BASIC TIMING PULSES (HORIZONTAL RATE)

Pulse Name	*Function*	*Delay of Pulse Leading Edge with Respect to Tape Horizontal Leading Edge (usec) ±10%*	*Pulse Width (usec ±10%*
Clock	Provides basic horizontal rate timing reference	0	0.5
Read X	Determines read time of capacitor memory	0.5	4.3
Sample	Closes sample switch on board 19	1.9	2.0
Ramp Reset	Closes ramp reset switch on board 19	3.2	0.7
Write	Closes write switch on board 14	8.5	32
Write X	Determines write time of capacitor memory	18.0	15
Clamp	Closes clamp switch on board 14	40.5	10*
V-Y Strobe	Determines times during which Y switches of VEC capacitor memory are closed	**	

* During line 1 only, clamp signal goes high for entire line period.

** V-Y Strobe signal is generated by OR gating Read X and Write X pulse and therefore goes high during both Read X and Write X pulse periods.

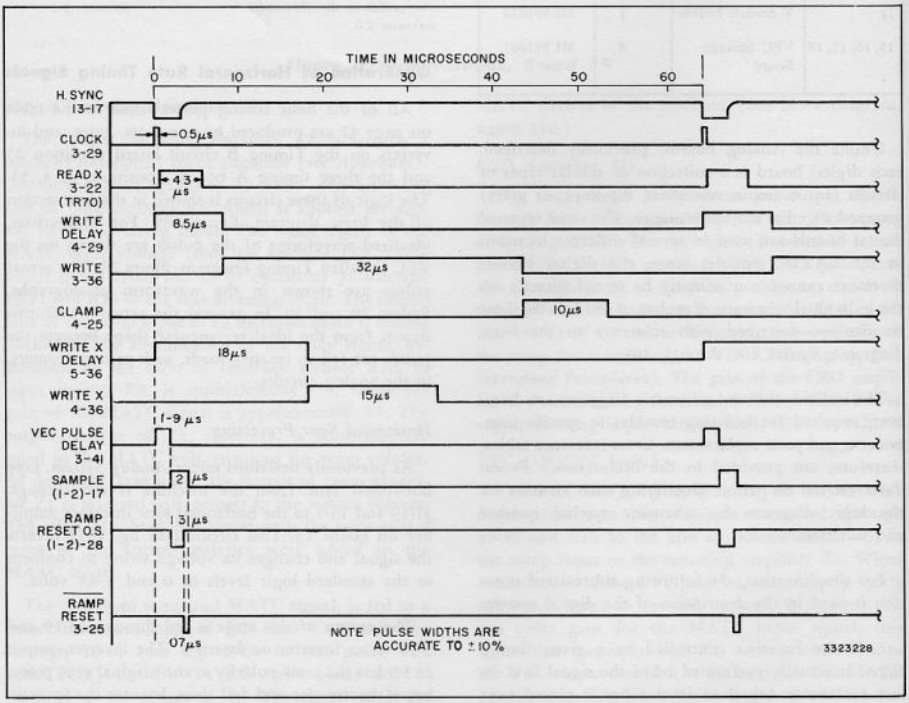


Figure 28—Detailed Timing Diagram of VEC Horizontal Rate Pulses

Terminal 3-9 is connected to 2-18 and 3. The path between 2-18 and 2-20 (shown dotted in figure 105) is completed by a jumper on the timing B board. From 2-20 the inverter output is fed through 3-31 to the input of the Clock one-shot on board 3.

Clock Pulse

At the leading edge of horizontal sync, the Clock one-shot on board 3 produces a negative going 0.5 microsecond pulse at 3-34 and a positive going 0.5 microsecond pulse at 3-29. The positive going pulse is used as a timing reference for the Read X pulse, the line counter advance, the Counter Reset pulse, and the Write 16 pulse. The negative going pulse is used as a reference for the VEC Pulse Delay and Write Delay one shots.

Read X Pulse

The positive going Clock pulse from 3-29 is fed through pin 33 of the Timing B module to the input of the Read X one shot.

At the trailing edge of the Clock pulse (0.5 microseconds after the leading edge of horizontal sync) the Read X one shot is triggered, and a negative going pulse, 4.3 microseconds wide, therefore, appears at its "0" output (2-34). This pulse is fed through 3-24 to an inverter on board 3. The output of the inverter, which constitutes the Read X pulse, is fed through 3-22 to the X Decoder circuits on boards 8, 9, 10, and 11, where it is combined with the outputs of the counter to form the VX control pulses for addressing the capacitor memory.

The negative going 4.3 microsecond pulse from the "0" output of the Read X one shot is also fed through 5-15 to a gate where it is combined with the Write X pulse to form the V-Y strobe signal, described later.

$\overline{\text{Sample}}$ and Ramp Reset Pulses

The negative going output of the Clock one shot, from 3-34, is applied through 3-43 to the trigger input of the VEC pulse delay one shot. The pulse width of this circuit is determined by potentiometer R5 in series with capacitor C8. (See schematic diagram of Timing A board, fig. 115). C8 is connected to ground by a jumper between pins 14 and 21 of the Timing B board, shown in dotted lines in figure 105. R5 is adjusted for a pulse width of 1.9 microseconds.

The positive going output of the VEC Pulse Delay one shot, at 3-41, is applied through 2-19 of the Timing B board to the trigger input of the Sample one-shot and through 2-26 of the Timing B board to the trigger input of the Ramp Reset one-shot.

At the end of the VEC pulse delay period, both the Sample and Reset one shots are triggered. The Sample pulse one shot then produces a positive going 2 microsecond pulse at 2-17 and the Reset one-shot produces a negative going 1.3 microsecond pulse at 2-28.

The sample pulse one shot output is fed through 2-8 to an inverter. The output of the inverter at 2-9, which constitutes the $\overline{\text{Sample}}$ pulse, is a negative going 2 microsecond pulse. This pulse is fed through 19-45 to the sample switch on board 19.

The negative going 1.3 microsecond pulse from the Ramp Reset one shot at 2-28 is fed through 3-28 to one input of a NAND gate. The positive going 2 microsecond pulse from the Sample pulse one shot at 2-17 is fed through 3-27 to the second input of the same gate. As explained in the *Appendix*, the output of a NAND gate is high except when all inputs are high. Both inputs are high only during the last 0.7 microseconds of the Sample pulse period, because the Ramp Reset one-shot output is low for the first 1.3 microseconds. The output of the gate, at 3-25, therefore, consists of a negative going 0.7 microsecond pulse. This pulse s applied through 19-35 to the Ramp Reset switch on board 19.

Write Pulse

The negative going output of the Clock one-shot at 3-34 is fed through 4-31 to the Write Delay one-shot, which produces an 8.5 microsecond positive going pulse at 4-29 and an 8.5 microsecond negative going pulse at 4-34. The negative going pulse is fed to the Write X Delay one-shot, which is described later under *Write X Pulse*. The positive going output is fed through 3-35 to the Write one-shot.

The trailing edge of the 8.5 microsecond input pulse triggers the Write one-shot, which has a 32 microsecond period. The negative going output pulse of the Write one-shot, at 3-38 is fed through 4-11 to an inverter, which produces a positive going pulse at 4-9. This signal, which constitutes the Write pulse, is fed through 14-5 to the Write switch on board 14.

Clamp Pulse

The positive going output of the Write one-shot, at 3-36 is fed through 2-44 to the Clamp one-shot on the Timing B module. At the trailing edge of the Write pulse, the Clamp one-shot produces a negative 10 microsecond pulse at 2-43. This pulse is fed through 4-27 to one input of an OR gate. The $\overline{L1}$ signal (described under *Line Counter*) from 6-35 is applied through 4-28 to the other input of the OR gate. The output of this gate, which constitutes the Clamp Drive signal is fed from 4-25 through 14-45 to the Clamp switch on board 14.

The $\overline{L1}$ signal is low throughout line 1 of the four head scanning periods. Consequently, the clamp drive signal is high and the clamp switch is closed for the entire period of line 1. This prevents the large MATC voltage excursion between the last line of each head scan and the first line of the next head scan (which does not represent a true velocity error difference) from reaching the memory drive amplifier.

During any line except the first, the $\overline{L1}$ signal is high, and the gate output level is determined by the other input of the gate. The clamp drive signal, therefore, goes high only during the 10 microsecond period of the negative going clamp pulse applied to that input.

NOTE: The Clamp one-shot also provides signals for CAC which are described under *Detailed Descriptions of CAC.*

Write X Pulse

The negative going output of the Write Delay one shot at 4-34 is fed through 5-35 to the Write X Delay one-shot, which produces an 18 microsecond positive going pulse at 5-36. This pulse is fed through 4-35 to the Write X one-shot.

At the trailing edge of the input pulse, the Write X one-shot produces a 15 microsecond positive going pulse. This pulse is fed from 4-36 through 4-15 to one input of a NAND gate. The purpose of this gate is to inhibit generation of the Write X pulse for a period of approximately 14 horizontal lines (830 microseconds) during each vertical interval. The inhibition is accomplished by applying a negative going pulse having a width of 14H (830 microseconds) to the other input of the NAND gate, 4-13, at the leading edge of the vertical pulse or 9H pulse. The 14H pulse is obtained from a one-shot on the Timing B module which provides an output signal on 2-39. This one shot is triggered by the output (from 13-4) of the Vertical Sync interface amplifier on board 13. (See description of board 13 under *Analog Circuits.)*

The output of the NAND gate at 4-14 is low only when both inputs are high. This simultaneously high condition occurs once per line, during the 15 microsecond period of the Write X one shot, except during the 14H portion of the vertical interval, when the gate output is high. The gate output is fed through 5-24 to an inverter. The inverter output at 5-22, which constitutes the Write X signal, is fed to the X decoding circuits on boards 7 through 11, where it is combined with the counter outputs to form the VX memory address signals.

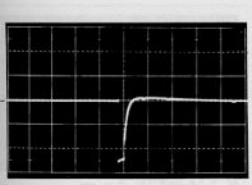
V-Y Strobe

The positive going Write X signal from 5-22, is also applied through 4-21 to a NAND gate, where it is combined with the $\overline{L1}$ signal from 6-38. As previously mentioned, the $\overline{L1}$ signal goes low only at the start of line 1 in each head scan and returns to the high level at the start of line 2. The gate output signal, at 4-22, therefore goes low during each Write X period, except in line 1. This signal is fed though 5-13 to one input of an OR gate. The other input to the OR gate, at 5-15, is a pulse from the Read X one-shot at 2-34 which goes low during the Read X period. The resulting output at 5-14, which is the V-Y strobe signal, is high for the Read X interval of the first line, and for both the Write X and Read X intervals of each succeeding line, except during the period of the Vertical Interval one-shot, (see figure 31). During this period, the V-Y strobe contains only Read X pulses, because, as previously described, the Write X pulses are inhibited.

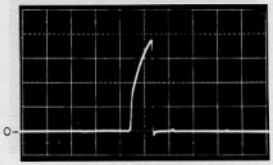
The V-Y strobe signal is fed from 5-14 through 12-37 to the Y decoder circuits. In these circuits the signal is combined with the 2X1 and 4X2 signals to produce the VY memory address signals.

Basic Timing Signals Derived from 4X2 and 2X1 Switcher Signals

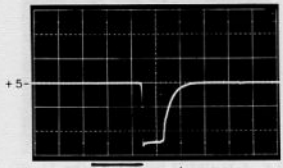
In addition to the timing signals based on horizontal sync, a number of timing signals based on the 2X1 or 4X2 switching pulses are generated on boards 3 through 7, which are described in the following paragraphs.



A. 3-31, 2 v/cm, 2 usec/cm
HOR IN TO CLOCK O.S.

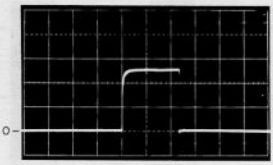


B. 3-29 (CLOCK), 1 v/cm
0.5 usec/cm

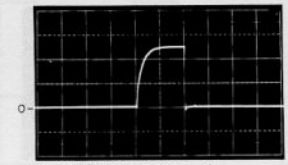


C. 3-34 $\overline{\text{(CLOCK)}}$, 2 v/cm
0.5 usec/cm

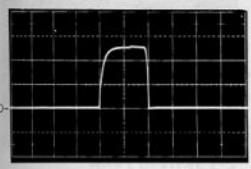
D. 2-34 $\overline{\text{(READ X)}}$, 2 v/cm
2 usec/cm
TR-70



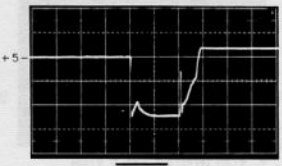
E. 3-22 (READ X), 2 v/cm
2 usec/cm



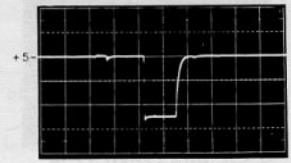
F. 3-41 (VEC DELAY), 2 v/cm
1 usec/cm



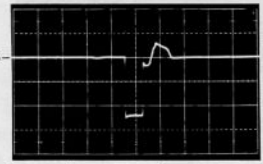
G. 2-17 (VEC SAMPLE), 2 v/cm
1 usec/cm



H. 2-9 (VEC $\overline{\text{SAMPLE}}$), 2 v/cm
1 usec/cm

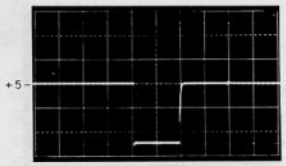


I. 2-28 (RAMP RESET), 2 v/cm
1 usec/cm

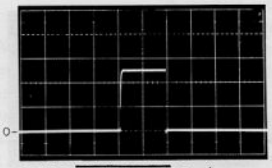


J. 3-25 $\overline{\text{(RAMP RESET)}}$, 2 v/cm
1 usec/cm

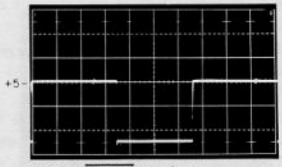
Figure 29—Waveforms, Horizontal Rate Timing Pulses



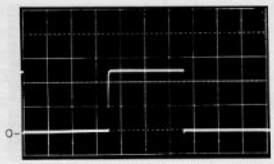
K. 4-34 (WRITE DELAY), 2 v/cm
5 usec/cm



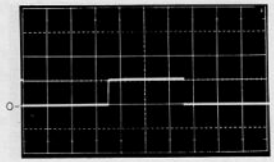
L. 4-29 (WRITE DELAY), 2 v/cm
5 usec/cm



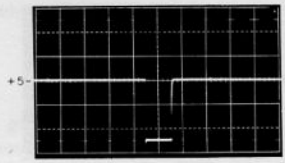
M. 3-38 (WRITE), 2 v/cm
10 usec/cm



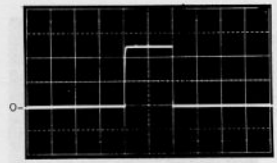
N. 3-36 (CLAMP O.S. TRIG.), 2 v/cm
10 usec/cm



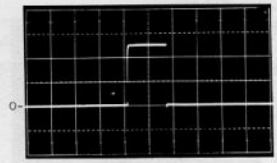
O. 4-9 (WRITE), 2 v/cm
10 usec/cm



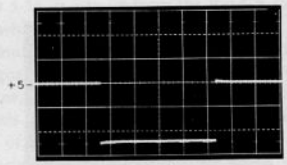
P. 2-43 (CLAMP O.S. "0"), 2 v/cm
10 usec/cm



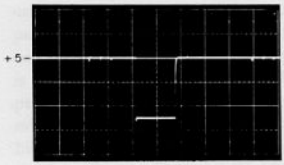
Q. 5-36 (WRITE X DELAY), 2 v/cm
10 usec/cm



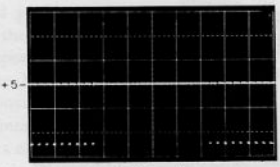
R. 4-36 (WRITE X PW) 2 v/cm
10 usec/cm



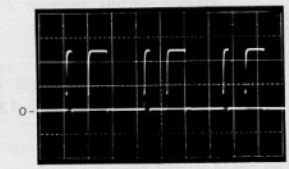
S. 2-39 (14 H) 2 v/cm
0.2 msec/cm



T. 4-14 (WRITE X) 2 v/cm
10 usec/cm



U. 4-14 (WRITE X) 2 v/cm
0.2 msec/cm



V. 5-14 (V-Y STROBE) 2 v/cm
20 usec/cm

Figure 30—Waveforms, Horizontal Rate Timing Pulses (Continued)

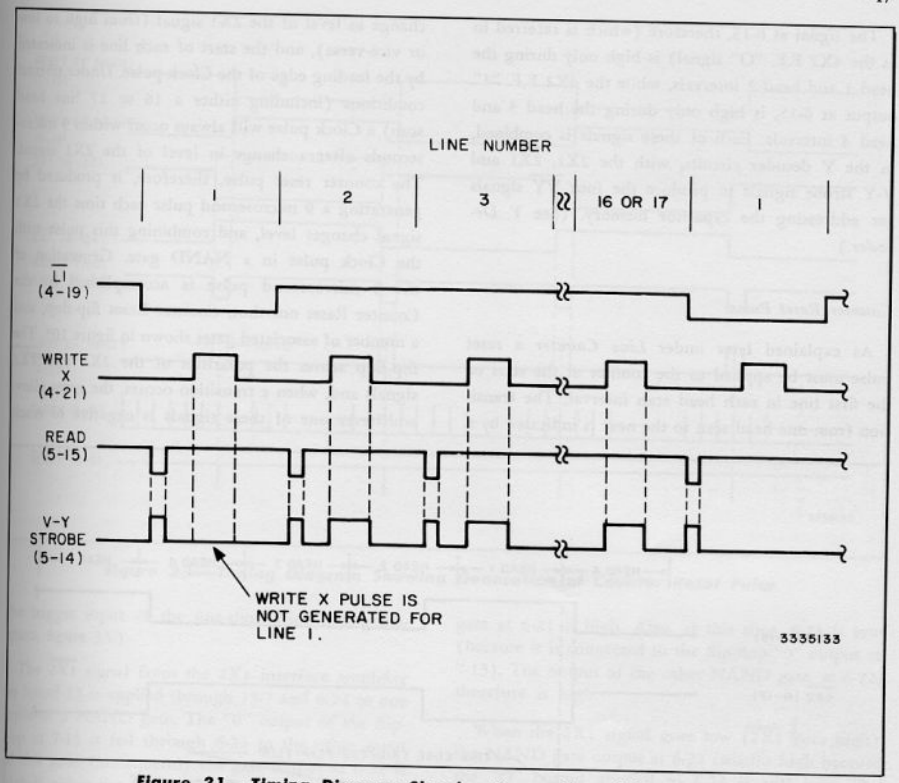


Figure 31—Timing Diagram Showing Generation of V-Y Strobe

4X2 Flip-Flop Signal

The 4X2 flip-flop on board 6 (see fig. 105) produces two output signals, one at 6-15, and the other at 6-13, which are used in the Y decoder circuits on board 12 to identify the four head scanning intervals. The generation of these signals is shown in the timing diagram, figure 32.

The output of the 2X1 signal interface amplifier on board 13 (previously described under *Analog Circuits*) is fed from 13-7 through 6-18 to the trigger input of the 4X2 flip-flop. The output of the 4X2 signal interface amplifier on board 13 is fed from 13-13 through 6-17 to one steering input of the flip-flop. In addition, the $\overline{4X2}$ signal from 13-13 is fed through 5-8 to an inverter, and the inverter output at 5-7, is fed through 6-14 to the other steering input of the flip-flop. Since the signal applied to the trigger input is inverted with respect to the 2X1 signal obtained from the tape machine, it is referred to as the $\overline{2X1}$ signal. Similarly, the steering voltage applied to 6-17 is called the $\overline{4X2}$ signal, while the opposite steering voltage applied to 6-14 is called the 4X2 signal.

At the start of the head 1 scanning interval, the $\overline{2X1}$ signal goes low and the 4X2 signal is high. Consequently (see description of flip-flop in *Appendix*), the flip-flop is triggered into the "0" state (6-13 high and 6-15 low). At the start of the head 2 interval, the $\overline{2X1}$ signal goes high, but the flip-flop is not triggered. At the start of the head 3 interval, however, the $\overline{2X1}$ signal again goes low, and, since the 4X2 signal is now high, the flip-flop is triggered into the "1" state (6-15 high and 6-13 low). The flip-flop remains in this state until the start of the head 1 interval in the next headwheel revolution.

The signal at 6-13, therefore (which is referred to as the 4X2 F.F. "O" signal) is high only during the head 1 and head 2 intervals, while the 4X2 F.F. "1" output at 6-15, is high only during the head 3 and head 4 intervals. Each of these signals is combined, in the Y decoder circuits, with the 2X1, $\overline{2X1}$ and V-Y strobe signals to produce the four $\overline{VY}$ signals for addressing the capacitor memory. (See *Y Decoder.*)

Counter Reset Pulse

As explained later under *Line Counter* a reset pulse must be applied to the counter at the start of the first line in each head scan interval. The transition from one head scan to the next is indicated by a change in level of the 2X1 signal (from high to low or vice-versa), and the start of each line is indicated by the leading edge of the Clock pulse. Under normal conditions (including either a 16 or 17 line head scan) a Clock pulse will always occur within 9 microseconds after a change in level of the 2X1 signal. The counter reset pulse, therefore, is produced by generating a 9 microsecond pulse each time the 2X1 signal changes level, and combining this pulse with the Clock pulse in a NAND gate. Generation of the 9 microsecond pulse is accomplished by the Counter Reset one-shot, Counter Reset flip-flop, and a number of associated gates shown in figure 105. The flip-flop senses the polarities of the 2X1 and $\overline{2X1}$ signals and, when a transition occurs, the gates allow whichever one of these signals is negative to reach

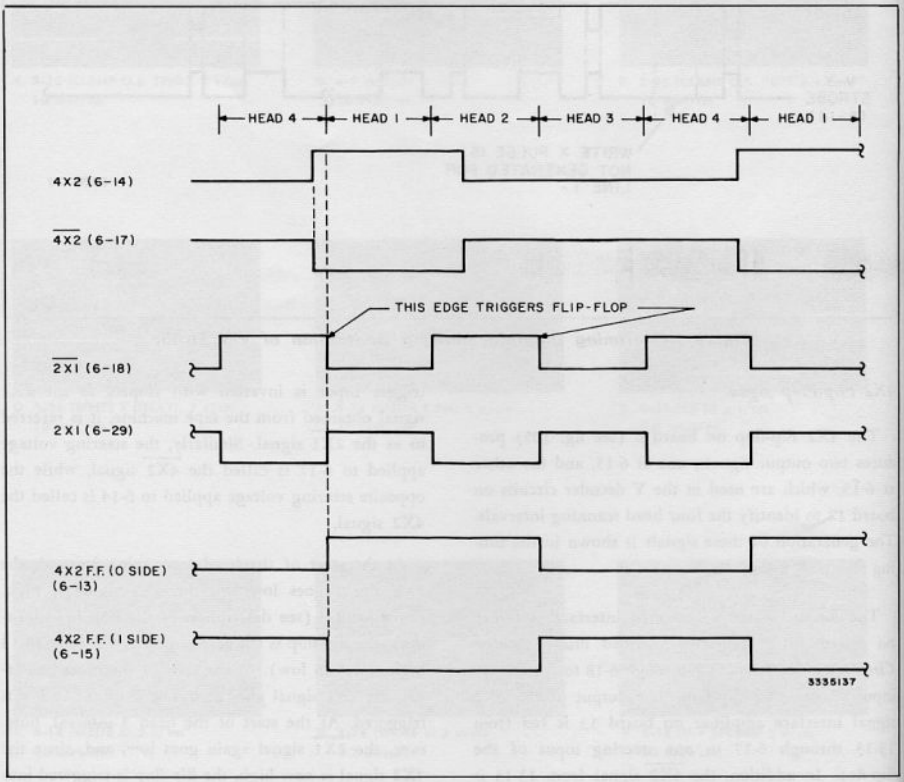


Figure 32—Timing Diagram Showing Generation of 4X2 Flip-Flop Pulses

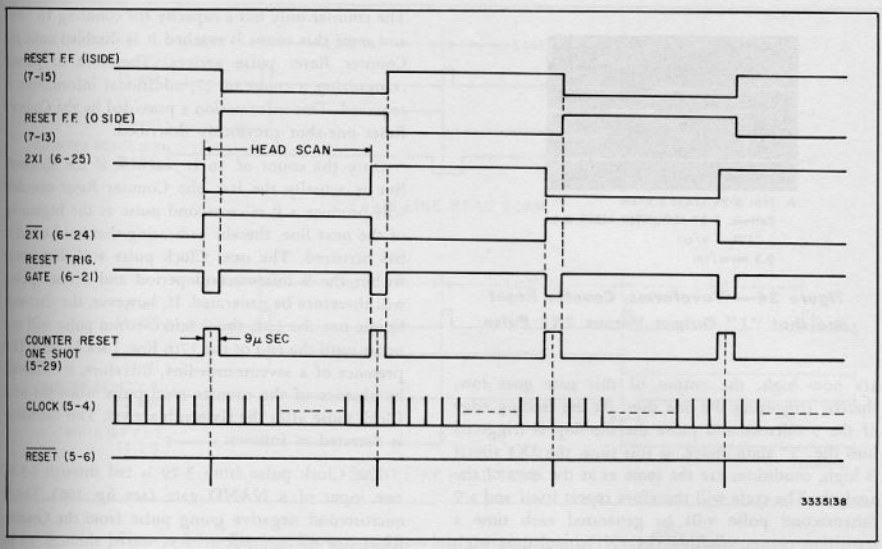


Figure 33—Timing Diagram Showing Generation of Counter Reset Pulse

the trigger input of the one-shot. (See timing diagram, figure 33.)

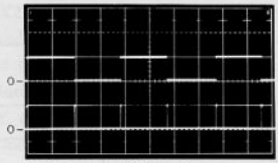
The $\overline{2X1}$ signal from the 2X1 interface amplifier on board 13 is applied through 13-7 and 6-24 to one input of a NAND gate. The "0" output of the flip-flop at 7-13 is fed through 6-23 to the other input of this gate. Consequently the gate output at 6-22 is high if either the $\overline{2X1}$ signal, or the flip-flop output at 7-13 is low. The NAND gate output is fed directly to one input of an OR gate on the same board, called the Reset Trigger gate. The output of this gate at 6-21 is fed to the trigger input of the Reset one-shot through 5-31.

The other input to the Reset Trigger gate is obtained from a second NAND gate through 6-27. The two inputs to this NAND gate consist of the 2X1 signal obtained by inverting the $\overline{2X1}$ signal, and the flip-flop "1" output from 7-15. The output of this NAND gate is high when either the 2X1 signal or the flip-flop "1" output is low.

To see how the circuit functions assume first that the Reset Flip-Flop is in the "1" state (7-15 high and 7-13 low) and that the 2X1 signal applied to 6-25 is high. Under these conditions, since both 6-25 and 6-28 are high the output of the NAND gate at 6-27 is low. Consequently, since 6-27 is connected to one input of the Reset Trigger gate, the output of this gate at 6-21 is high. Also, at this time, 6-23 is low (because it is connected to the flip-flop "0" output at 7-13). The output of the other NAND gate, at 6-22, therefore is high.

When the 2X1 signal goes low ($\overline{2X1}$ goes high) the NAND gate output at 6-22 remains high because the "O" output applied to 6-23 is still low. The NAND gate output at 6-27, goes high because the $\overline{2X1}$ input to this gate at 6-25 goes low. Consequently, since both inputs to the Reset Trigger gate are now high, its output at 6-21 goes low, thereby triggering the Counter Reset one-shot. This circuit then produces a 9 microsecond negative going pulse at 5-34 and a 9 microsecond positive going pulse at 5-29. At the end of the pulse period, the trailing edge of the pulse at 5-29 triggers the flip-flop into the "0" state (7-13 high, 7-15 low). Under these conditions, since the $\overline{2X1}$ input to the NAND gate at 6-24 is high, and the flip-flop "0" output applied to 6-23 is also high, the output of this gate is low. The output of the Reset Trigger gate at 6-21, therefore, is high.

When the next head scan transition occurs, the $\overline{2X1}$ signal goes low and the NAND gate output at 7-22, therefore goes high. At this time, the output of the other NAND gate at 6-27 is high, because the flip-flop "1" output applied to 6-28 is low. Consequently since both inputs to the Reset Trigger gate



A. Top: 6-29 (2X1) 5 v/cm
Bottom: 5-29 (COUNTER RESET O.S. "1"), 5 v/cm
0.5 msec/cm

Figure 34—Waveforms, Counter Reset one-shot "1" Output Versus 2X1 Pulse

are now high, the output of this gate goes low, thereby triggering the one shot. At the trailing edge of the 9 microsecond pulse the flip-flop is triggered into the "1" state. Since, at this time, the 2X1 signal is high, conditions are the same as at the start of the analysis. The cycle will therefore repeat itself and a 9 microsecond pulse will be generated each time a transition occurs, whether the 2X1 signal goes high or low. (See waveforms in figure 34.)

The 9 microsecond positive going pulse from the one-shot output at 5-29 is applied to one input of a NAND gate at 5-3 and the Clock pulse from 3-29 is applied to the other input of this gate at 5-4. When the 9 microsecond pulse is not present, 5-3 is low. The Clock pulses, therefore, have no effect and the gate output at 5-6 remains high. When, however, the 9 microsecond pulse occurs, 5-4 goes high, thereby enabling or priming the gate. The next Clock pulse to occur will normally fall within the 9 microsecond period. When the Clock pulse arrives the output at 5-6 will go low, thereby producing the Counter Reset pulse. This pulse is fed to the counter at 7-43 where it restores the counter to the state corresponding to the first count. (See *Line Counter.*)

Write 16 Pulse

As previously mentioned in the *Functional Description,* some of the head scan intervals contain 17 lines, but only 16 capacitors are provided in the memory bank, for each interval. The sixteenth capacitor must be written into only during the seventeenth line. To accomplish this, a signal called the Write 16 pulse is required, as explained under *X Decoder.* The Write 16 pulse goes high only at the start of a seventeenth line, and remains high for the duration of the line.

To permit generating the Write 16 pulse some means of recognizing a seventeenth line is required. The counter only has a capacity for counting 16 lines, and once this count is reached it is disabled until the Counter Reset pulse arrives. Therefore to permit recognizing a count of 17, additional information is required. This information s provided by the Counter Reset one-shot previously described.

Once the count of 16 is reached, if the sixteenth line is actually the last, the Counter Reset one-shot will produce a 9 microsecond pulse at the beginning of the next line, thereby indicating that head transfer has occurred. The next Clock pulse will then occur within the 9 microsecond period and a reset pulse, will therefore be generated. If, however, the sixteenth line is not the last, the 9 microsecond pulse will not occur until the end of the 17th line. (See fig. 35.) The presence of a seventeenth line, therefore, is indicated by absence of the counter reset pulse when the next Clock pulse after the sixteenth arrives. This condition is detected as follows:

The Clock pulse from 3-29 is fed through 3-5 to one input of a NAND gate (see fig. 105). The 9 microsecond negative going pulse from the Counter Reset one-shot output at 5-34 is fed through 3-8 to the other input of the gate. The gate output at 3-7 therefore will normally go low during each Clock pulse, but will remain high whenever the 9 microsecond pulse is present. The gate output is fed through 3-4 to an inverter, and the inverter output is fed through 3-6 and 4-5 to one input of another NAND gate. The second input to this NAND gate, applied at 4-8, is called the L16 signal.

The L16 signal is derived by decoding the outputs of the line counter as explained under *Line Counter.* This signal is normally low, but goes high whenever the counter indicates a count of 16. The gate output at 4-7, therefore is normally held high by the L16 signal and the gate is disabled. When the L16 signal goes high at the count of 16, the gate is enabled, but its output still remains high unless the input at 4-5 goes high at the next Clock pulse. In a 16-line head scan, the input at 4-5 will remain low because passage of the Clock pulse is inhibited by the 9 microsecond pulse applied to 3-8. In a 17 line head scan, however, this Clock pulse is not inhibited. The start of a seventeenth line therefore is indicated by the appearance of a single negative going Clock pulse at 4-7.

To generate the Write 16 pulse, the gate output at 4-7 is applied through 7-20 to the "Set" input of a Set-Reset flip-flop consisting of two cross coupled gates. (See *Appendix* for description of this circuit.) The Counter Reset pulse is applied through 7-23 to the "Reset" input of the flip-flop. To provide the

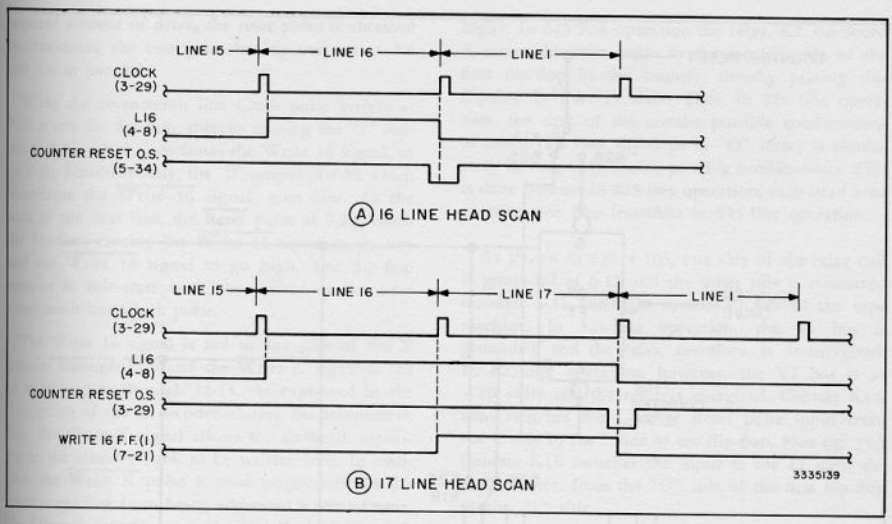


Figure 35—Timing Diagram Showing Generation of Write 16 Pulse

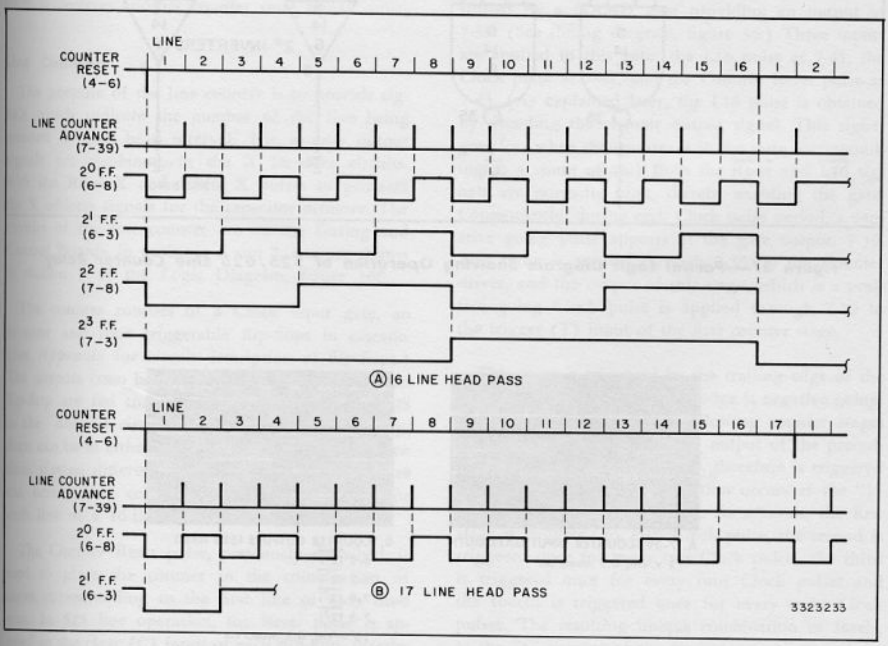


Figure 36—Simplified Timing Diagram Showing Line Counter Operation

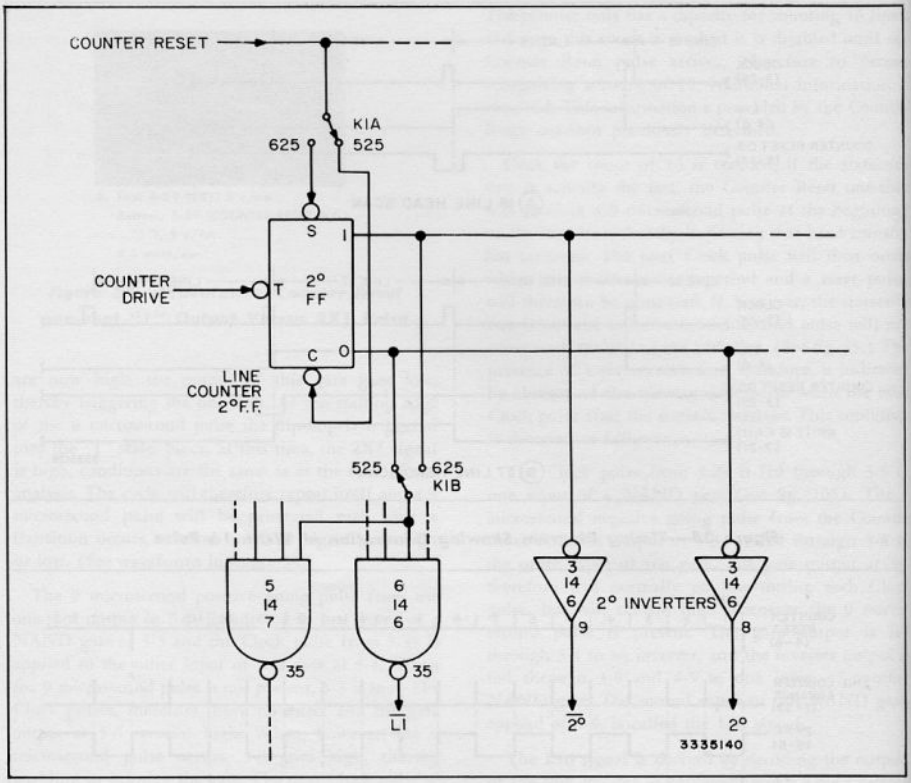
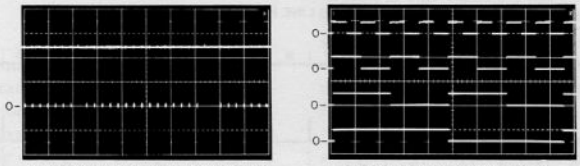


Figure 37—Partial Logic Diagram Showing Operation of 525/625 Line Counter Relay



A. 7-39 (COUNTER INPUT GATE OUT)
2 v/cm, 0.2 msec/cm

B. COUNTER OUTPUTS (525 lines)
6-9 $(\overline{2^0})$
6-5 $(\overline{2^1})$
7-9 $(\overline{2^2})$
7-5 $(\overline{2^3})$
10 v/cm, 0.1 msec/cm

Figure 38—Waveforms, Line Counter

required amount of drive, the reset pulse is obtained by connecting the two gates having outputs at 4-6 and 5-6 in parallel.

When the seventeenth line Clock pulse arrives at 7-20 it sets the flip-flop, thereby causing the "1" output at 7-21, which constitutes the Write 16 signal, to go high. Simultaneously, the "0" output at 7-22 which constitutes the $\overline{\text{Write 16}}$ signal, goes low. At the start of the next line, the $\overline{\text{Reset}}$ pulse at 7-23, resets the flip-flop, causing the $\overline{\text{Write 16}}$ signal to go low and the $\overline{\text{Write 16}}$ signal to go high. The flip-flop remains in this state until the arrival of the next seventeenth line Clock pulse.

The Write 16 signal is fed to one gate of the X decoder through 11-5 and the $\overline{\text{Write X}}$ signal is fed to another gate through 11-15. As explained in the description of the X decoder, during the seventeenth line, the Write X signal allows the sixteenth capacitor in the memory bank to be written into. In addition, the $\overline{\text{Write X}}$ pulse is used to prevent the fifteenth capacitor from being addressed a second time, the fifteenth capacitor would normally be addressed, because the counter still indicates a count of sixteen until it receives another counter reset signal.

Line Counter

The purpose of the line counter is to provide signals which indicate the number of the line being scanned in each head interval. The counter output signals are combined, in the X Decoder circuits, with the Read X and Write X pulses to generate the X address signals for the capacitor memory. The circuits of the line counter are on the Gating and Control Boards, in positions 6 and 7, and are shown in section 2 of the Logic Diagram, figure 106.

The counter consists of a Clock input gate, an inverter and four triggerable flip-flops in cascade. (See *Appendix* for circuit description of flip-flops.) The outputs from both the "0" and "1" side of each flip-flop are fed through driver amplifiers to gates in the decoder circuits. Since each of the four flip-flops can be in either of two possible states at a given time, sixteen different combinations of counter states can occur. One combination, therefore, exists for each line of a 16-line head scan.

The Counter Reset pulse, previously described, is used to place the counter in the combination of states corresponding to the first line of each head scan. In 525 line operation, the Reset pulse is applied to the clear (C) input of each flip-flop, thereby placing the flip-flop in the "O" state ("O" output high). In 625 line operation the relay, K1, on board 6, steers the reset pulse to the set (S) side of the first flip-flop in the counter, thereby placing this flip-flop in the "1" state. Thus, in 625 line operation, the first of the sixteen possible combinations of states (all four flip-flops in "O" state) is eliminated, leaving only fifteen possible combinations. This is done because in 625-line operation, each head scan contains one line less than in 525-line operation.

As shown in figure 106, one side of the relay coil is grounded at 6-12 and the other side is connected through 6-31 and J1-5 to the VI bus of the tape machine. In 525-line operation, the VI bus is grounded, and the relay, therefore, is de-energized. In 625-line operation, however, the VI bus is at −20 volts and the relay is energized. Contact K1A then switches the Counter Reset pulse input from the C side to the S side of the flip-flop. (See fig. 37.) Contact K1B switches the input to the L1 gate, described later, from the "O" side of the first flip-flop to the "1" side.

Admission of Clock pulses to the counter is controlled by a NAND gate providing an output at 7-39. (See timing diagram, figure 36.) Three inputs are applied to this gate: the L16 pulse at 7-41, the Clock pulse at 7-42, and the Counter Reset pulse at 7-43. (As explained later, the L16 pulse is obtained by decoding the counter output signal. This signal goes low when the counter is in the state corresponding to a count of 16.) Both the $\overline{\text{Reset}}$ and $\overline{\text{L16}}$ signals are normally high, thereby enabling the gate. Consequently, during each Clock pulse period, a negative going pulse appears at the gate output, 7-39. This pulse is applied through 7-30, to the Counter driver, and the output of this stage, which is a positive going Clock pulse is applied through 7-29 to the trigger (T) input of the first counter stage.

This stage is triggered by the trailing edge of the Clock pulse, since the trailing edge is negative going. The trigger inputs of the following counter stages are each connected to the "1" output of the preceding stage. Each of these stages, therefore is triggered when a negative going transition occurs at the "1" output of the preceding stage. As a result, the first stage is triggered by each Clock pulse, the second is triggered once for every two Clock pulses, the third is triggered once for every four Clock pulses and the fourth is triggered once for every eight Clock pulses. The resulting unique combination of levels, at the "1" outputs of the four stages corresponds to the number of each Clock pulse in a head scan as

shown in the table below. In this table and on the drawings, the first stage is identified by the number 2^0, the second by 2^1, the third by 2^2 and the fourth by 2^3. These symbols represent in powers of two, the number of Clock pulses which must occur before the corresponding stage is triggered.

LEVELS AT "1" SIDES OF COUNTER STAGES DURING EACH LINE COUNT

Levels				*Line Number*	
2^3	2^2	2^1	2^0	*525 Line Standard*	*625 Line Standard*
L	L	L	L	1	—*
L	L	L	H	2	1
L	L	H	L	3	2
L	L	H	H	4	3
L	H	L	L	5	4
L	H	L	H	6	5
L	H	H	L	7	6
L	H	H	H	8	7
H	L	L	L	9	8
H	L	L	H	10	9
H	L	H	L	11	10
H	L	H	H	12	11
H	H	L	L	13	12
H	H	L	H	14	13
H	H	H	L	15	14
H	H	H	H	16**	15***

* This state does not exist on 625-line standards.

** Counter held in this state if 17th line occurs.

*** Counter held in this state if 16th line occurs.

Note that both the "0" and "1" outputs of each Counter stage are fed out to individual inverter stages, although only the "1" outputs are shown in the table. The "1" output of each stage is identified on the drawings by the number of the stage (2^0, 2^1, 2^2, or 2^3.) The "0" output is identified by the same number with a bar over it ($\overline{2^0}$, $\overline{2^1}$, $\overline{2^2}$, $\overline{2^3}$). Each of the eight inverter outputs is fed to gates in the X decoder circuits, described later. In addition, the "1" outputs of the four stages are fed to one gate called the $\overline{\text{L16}}$ gate and the "0" outputs are fed to another called the $\overline{\text{L1}}$ gate. These gates are provided to permit identifying the first and the sixteenth count of each head scan (first and fifteenth count on 625-line standards).

The output of the $\overline{\text{L16}}$ gate at 6-39 is normally high because at least one of its four inputs is low. At the count of 16 (or 15 on 625 line standards) all of the inputs go high, and the output signal therefore goes low. This output, called the $\overline{\text{L16}}$ signal, is fed through 7-41 to the Counter input gate, and through 7-25 to an inverter. The output of the inverter at 7-27, called the L16 signal, is fed through 4-8, as previously described, to enable the Write 16 gate.

The $\overline{\text{L16}}$ signal applied to 7-41 disables the Counter Input gate by holding the gate output at 7-39 high at the count of 16. This prevents the seventeenth Clock pulse from reaching the Counter (if one occurs before the Counter Reset pulse occurs) and upsetting the counter state. When the Counter Reset pulse does occur, its leading edge immediately resets the flip-flops, and the $\overline{\text{L16}}$ signal goes high, removing the inhibition placed by this signal on the Counter Input gate. At the same time, however, the Counter Reset signal, applied to another input of the gate through 7-43, goes low thereby keeping the gate disabled until the end of the Counter Reset pulse. This prevents the Clock pulse applied to 7-42 during the Reset pulse time from falsely triggering the Counter at its trailing edge.

The $\overline{\text{L1}}$ signal is used in the Clamp Drive and V-Y Strobe circuits as explained in the descriptions of these circuits. On 525 line standards, the "0" outputs of all four flip-flops are applied to inputs of the $\overline{\text{L1}}$ gate. On 625 line standards, relay contact K1B switches the "1" side of the 2^0 counter to the gate instead of the "0" side. On either set of standards when the Counter Reset pulse occurs, thereby placing the counter in the line 1 condition, the output of the L1 gate at 6-35 goes low. The gate output remains low until the arrival of the next Clock pulse when it switches to the high level.

VX Decoder

As briefly explained in the *Functional Description* two signals are required to address a given capacitor in the VEC memory bank, the VX and $\overline{\text{VY}}$ signals. The $\overline{\text{VY}}$ signals causes a semiconductor switch to ground one side of the capacitor during the read and write times of every line in a particular one of the four head scan intervals. The VX signal causes a different switch to connect the other side of the capacitor to the I/O bus during the read time of one particular line in every head scan, and also during the write time of the following line.

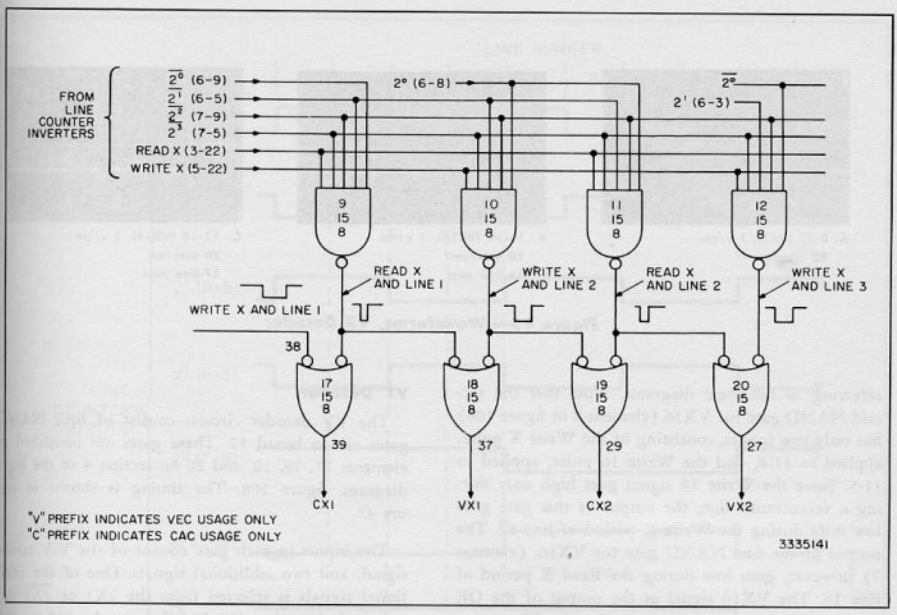


Figure 39—Partial Logic Diagram Showing VX1 VX2 Decoding Circuits

The VY signals are obtained by extracting (decoding) the required information from the 2x1, the 4x2 and V-Y strobe signals as described under *Y Decoder*. The VX signals are obtained by decoding the eight outputs of the line counter (2^0, 2^1, 2^2, 2^3, $\overline{2^0}$, $\overline{2^1}$, $\overline{2^2}$, $\overline{2^3}$), the Write X pulse and the Read X pulse in a number of gates as explained below.

The X decoder circuits for the VEC are contained on boards 8 through 11 and are shown in sections 2, 3, and 4, of the logic diagram, figure 106, 107, and 108. (These boards also contain the X decoder circuits for the CAC which are explained under *Detailed Description of CAC.)*

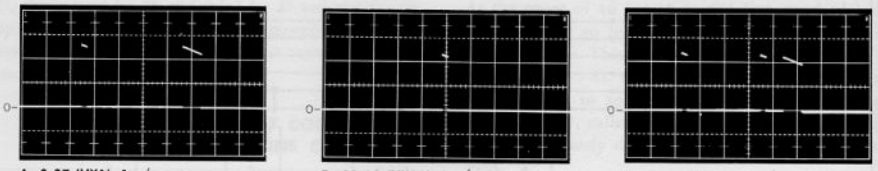
Since there are sixteen capacitors in the memory for each head scan, a total of 16 VX signals are generated (15 on 625 line standards). These signals are designated by the symbols VX1 through VX16. In general (except for VX16, described later) each signal goes high during the Read X period of one particular scanning line and also, during the Write X period of the next scanning line. For example VX1 goes high during the Read X pulse period of line 1 and during the Write X period of line 2. This is made to occur by using two NAND gates and an OR gate for each VX signal as shown in figure 39. (This figure also shows additional gates which are used only for CAC, and therefore should be ignored during this discussion.)

The two NAND gates for generation of VX1 are identified in figure 39 as elements 9 and 10, and the OR gate, as element 18. The inputs to the first NAND gate (element 9) consist of the Read X pulse, and the particular four outputs of the Counter that go high during line 1. (See timing diagram, figure 41.) The output of this gate therefore goes low only during the Read X period of line 1.

Similarly, the inputs to the second NAND gate (element 10) consist of the Write X pulse and the particular four outputs of the Counter that go high during line 2. The output of this gate, therefore goes low only during the Write X period of line 2.

The outputs of elements 9 and 10 are each applied to an input of the OR gate (element 8) for VX1. The output of this gate goes high when either input goes low. Consequently the VX1 signal goes high during the Read X period of line 1 and the Write X period of line 2. (See fig. 41).

Similar analyses hold for generation of all the other VX signals except VX16, as may be seen by



A. 8-37 (VX1), 1 v/cm
20 usec/cm

B. 11-10 (VX16), 1 v/cm
20 usec/cm
16-line pass

C. 11-10 (VX16), 1 v/cm
20 usec/cm
17-line pass

Figure 40—Waveforms, VX Decoder

referring to the logic diagrams. Note that the second NAND gate for VX16 (element 8 in figure 108) has only two inputs, consisting of the Write X pulse, applied to 11-8, and the Write 16 pulse, applied to 11-5. Since the Write 16 signal goes high only during a seventeenth line, the output of this gate goes low only during the Write X period of line 17. The output of the first NAND gate for VX16, (element 7) however, goes low during the Read X period of line 16. The VX16 signal at the output of the OR gate, 11-10, therefore, contains only a positive going Read X pulse during line 16. In a seventeen-line scan, however, the VX-16 signal contains a positive-going Read X pulse during lines 16 and 17 and also, a positive going Write X pulse during line 17. (See waveforms in figure 40).

Note that at the same time that the Write 16 pulse is applied to the second NAND gate (element 8) for the VX16 signal, the $\overline{\text{Write 16}}$ signal is applied, through 11-15 to the second NAND gate (element 6) for the VX15 signal. This negative going signal disables element 6 to prevent appearance of a Write X pulse in the VX15 signal during line 17. If the gate were not disabled, its output would go low during the Write X period of line 17, because the counter output signals applied to its input remain high during line 17 as well as line 16. (This condition occurs because the counter is held in the count 16 condition during line 17.)

NOTE: On 625 line standards, the Counter starts each head scan in the condition representing the count of 2. The initial state of the counter produces VX2. Each of the VX2 through VX16 signals, therefore, goes high one line count earlier than in 525 line standards. For example, VX2 goes high during the Read X period of line 1 and the Write X period of line 2, instead of the corresponding periods of lines 2 and 3.

VY Decoder

The VY decoder circuits consist of four NAND gates all on board 12. These gates are identified as elements 17, 18, 19, and 20 on section 4 of the logic diagram, figure 108. The timing is shown in figure 42.

The inputs to each gate consist of the V-Y strobe signal, and two additional signals. One of the additional signals is selected from the 2X1 or $\overline{\text{2X1}}$ signals and the other is selected from the "1" or "0" outputs of the 4X2 Flip-flop. (These signals are derived as explained under *Basic Timing Signals Derived from 4X2 and 2X1 Switcher Signals.*)

As previously mentioned, the 4X2 Flip-Flop "0" output goes high during the scanning periods of heads 1 and 2 while the 2X1 signal goes high during the scanning periods of heads 1 and 3. Therefore these two signals are simultaneously high only during the head 1 interval. Similarly, the 2X1 signal and the 4X2 flip-flop "0" outputs are simultaneously high only during the head 2 interval. In this manner, four unique pairs of signals, can be selected each of which is high only during a particular one of the four head scans, as shown in the following table.

VY DECODER INPUT SIGNALS

Signals Simultaneously High	*Head Scan Interval*
2X1 and 4X2 F.F. "0"	1
$\overline{\text{2X1}}$ and 4X2 F.F. "0"	2
2X1 and 4X2 F.F. "1"	3
$\overline{\text{2X1}}$ and 4X2 F.F. "1"	4

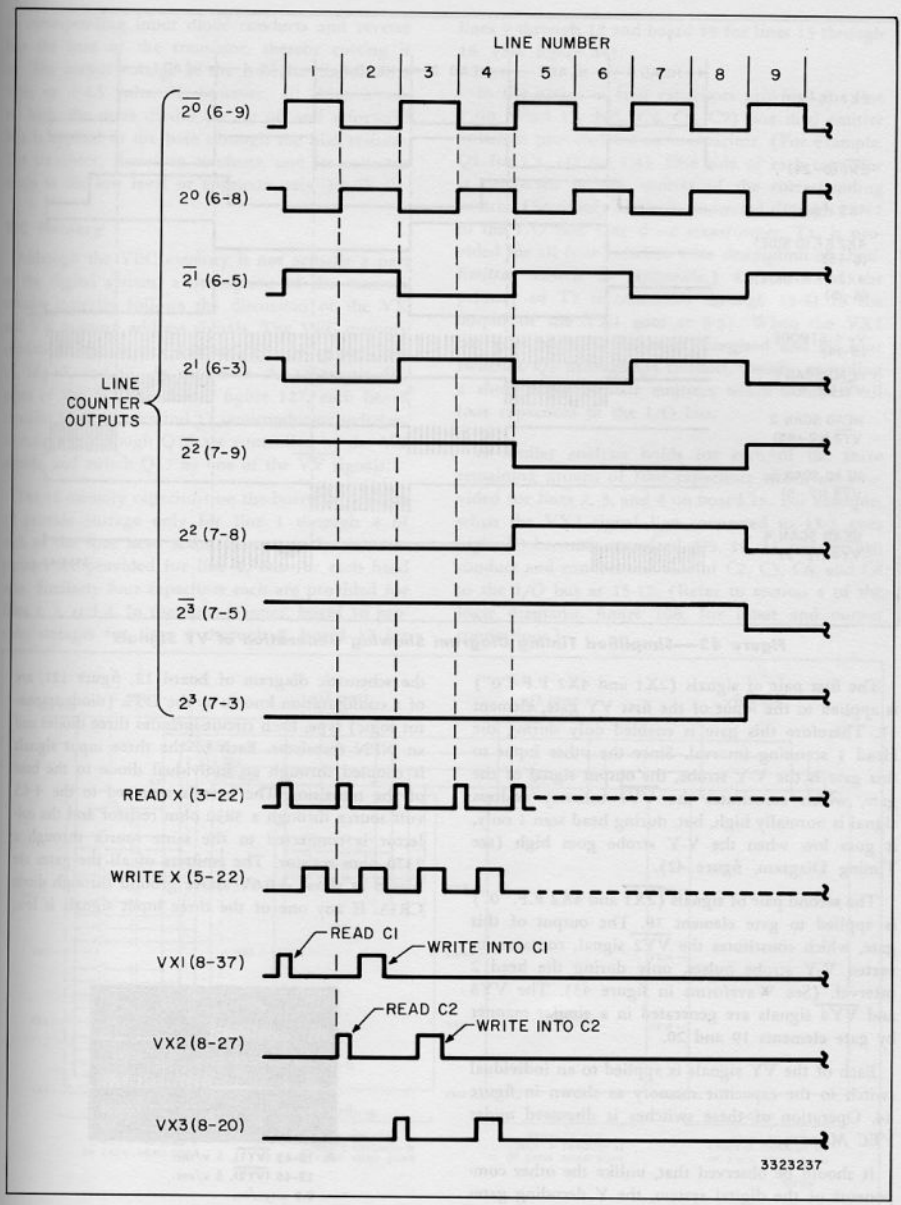


Figure 41—Timing Diagram Showing Generation of VX Signals

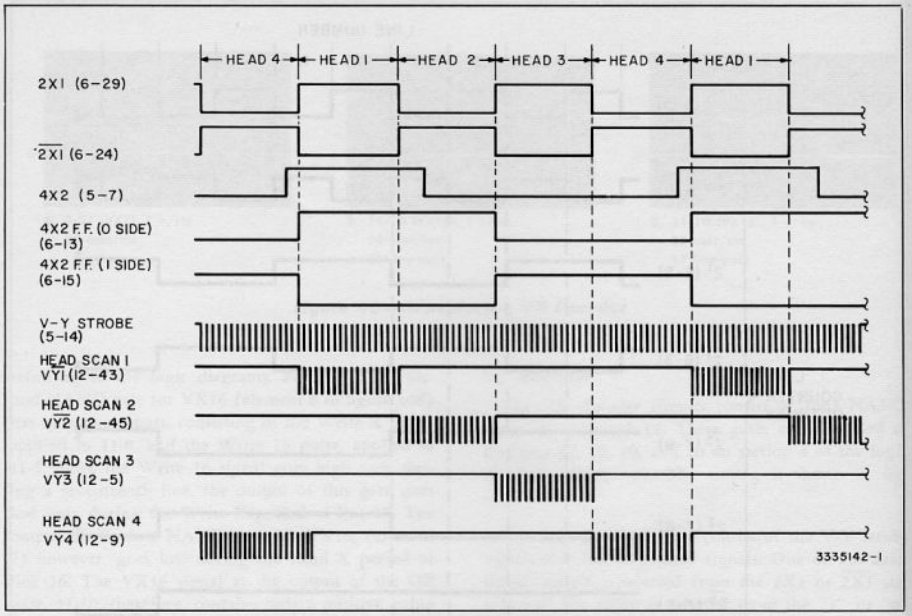


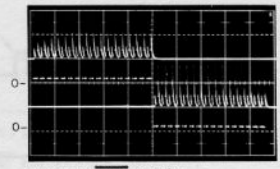
Figure 42—Simplified Timing Diagram Showing Generation of VY Signals

The first pair of signals (2X1 and 4X2 F.F. "0") is applied to the input of the first VY gate, element 17. Therefore this gate is enabled only during the Head 1 scanning interval. Since the other input to this gate is the V-Y strobe, the output signal of the gate, which constitutes the $\overline{VY1}$ memory address signal is normally high, but, during head scan 1 only, it goes low when the V-Y strobe goes high (see Timing Diagram, figure 42).

The second pair of signals ($\overline{2X1}$ and 4X2 F.F. "0") is applied to gate element 18. The output of this gate, which constitutes the $\overline{VY2}$ signal, contains inverted V-Y strobe pulses, only during the head 2 interval. (See Waveforms in figure 43). The $\overline{VY3}$ and $\overline{VY4}$ signals are generated in a similar manner by gate elements 19 and 20.

Each of the $\overline{VY}$ signals is applied to an individual switch in the capacitor memory as shown in figure 44. Operation of these switches is discussed under *VEC Memory.*

It should be observed that, unlike the other components of the digital system, the Y decoding gates on board 12 consist of discrete components instead of integrated circuits. The gate circuits, shown on the schematic diagram of board 12, figure 121, are of a configuration known as the DTL (diode-transistor logic) type. Each circuit includes three diodes and an NPN transistor. Each of the three input signals is coupled through an individual diode to the base of the transistor. The base is returned to the +4.5 volt source through a 3830 ohm resistor and the collector is connected to the same source through a 2370 ohm resistor. The emitters of all the gates are biased at about +0.6V above ground through diode CR13. If any one of the three input signals is low,



A. 12-43 $\overline{(VY1)}$, 5 v/cm
12-45 $\overline{(VY2)}$, 5 v/cm
0.2 msec/cm

Figure 43—Waveforms, VY Decoder

its corresponding input diode conducts and reverse bias the base of the transistor, thereby cutting it off. The output voltage at the collector therefore is high, or +4.5 volts. If, however, all three inputs are high, the three diodes are cut off and a forward bias is applied to the base through the bias resistor. The transistor, therefore conducts, and its collector drops to the low level or approximately +0.6V.

VEC Memory

Although the VEC memory is not actually a part of the digital system, a description of the memory circuits logically follows the discussion of the VX and $\overline{VY}$ memory address signals. The VEC memory consists of four identical boards occupying positions 15, 16, 17, and 18. As shown in the schematic diagram of the Storage Board, figure 127, each board contains 16 capacitors and 17 semiconductor switches. Switches Q1 through Q16 are controlled by the VX signals, and switch Q17 by one of the $\overline{VY}$ signals.

The 16 memory capacitors on the board in position 15 provide storage only for line 1 through 4 of each of the four head scans. Consequently, four capacitors are provided for line 1, one for each head scan. Similarly four capacitors each are provided for lines 2, 3, and 4. In the same manner, board 16 provides storages for lines 5 through 8, board 17 for lines 9 through 12 and board 18 for lines 13 through 16. (See figure 44).

In the group of four capacitors provided for line 1 on board 15, (C1, C4, C5, C7) one dual emitter switch is provided for each capacitor. (For example, Q1 for C1, Q2 for C4). One side of each capacitor is connected to one emitter of the corresponding switch. The other emitter is connected through 15-17 to the I/O bus. One drive transformer, T1, is provided for all four switches. (See description of *Dual-Emitter Switch* in *Appendix*.) One side of the primary of T1 is connected through 15-41 to the output of the VX1 gate at 8-37. When the VX1 bus goes high, T1 becomes energized and all four switches, Q1 through Q4 conduct, thereby providing a short between their emitters which connects all four capacitors to the I/O bus.

A similar analysis holds for each of the three remaining groups of four capacitors which are provided for lines 2, 3, and 4 on board 15. For example, when the VX2 signal line connected to 15-3 goes high, T3 becomes energized. Q9, 10, 11 and 12 then conduct and connect one side of C2, C3, C6, and C8 to the I/O bus at 15-17. (Refer to section 4 of the logic diagrams, figure 108, for input and output connections.)

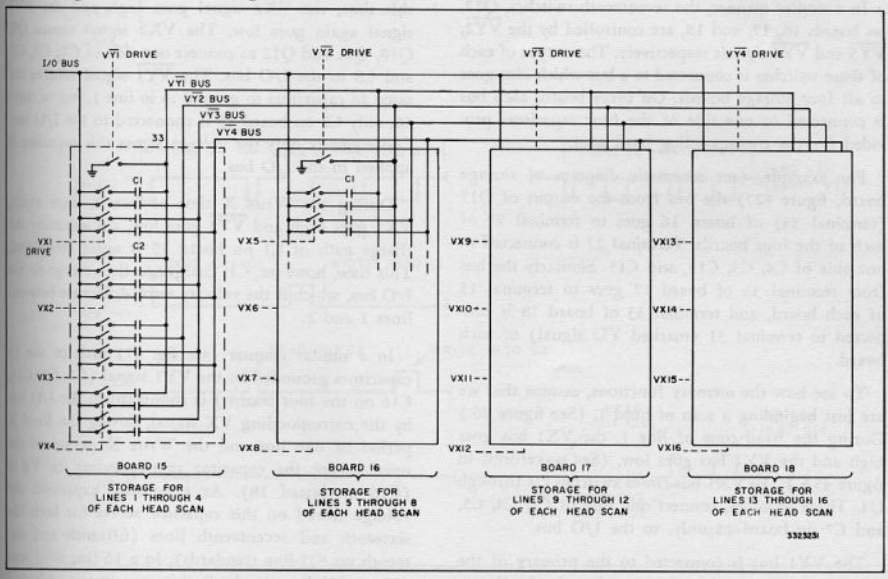
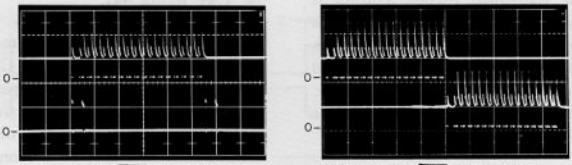


Figure 44—VEC Memory Organization



A. Top: 15-43 ($\overline{VY1}$ IN) 5 v/cm
Bottom: 15-41 (VX1 IN) 5 v/cm
0.2 msec/cm

B. Top: 15-43 ($\overline{VY1}$ IN), 5 v/cm
Bottom: 16-43 ($\overline{VY2}$ IN), 5 v/cm
0.2 msec/cm

Figure 45—Waveforms, VEC Memory

The seventeenth switch on board 15, Q17, is controlled by the $\overline{VY1}$ signal which is fed from 12-43 through 15-43, to the primary of drive transformer T5. One emitter of Q17 is grounded, and the other emitter is connected through 15-33 to a bus which goes to terminal 13 of each of the four storage boards in positions 15, 16, 17, and 18. Terminal 13 on each board is connected to one side of the particular capacitor in each group of four, which is provided for head scan number 1 (C1, C2, C14, C16). The side of each capacitor connected to terminal 13 is opposite to the one connected to the corresponding VX switch.

In a similar manner, the seventeenth switches, Q17, on boards 16, 17, and 18, are controlled by the $\overline{VY2}$, $\overline{VY3}$ and $\overline{VY4}$ signals respectively. The output of each of these switches is connected to a bus which also goes to all four storage boards. On every board, each bus is connected to one side of the four capacitors provided for the corresponding head scan.

For example, (see schematic diagram of storage board, figure 127) the bus from the output of Q17 (terminal 33) of board 16 goes to terminal 27 of each of the four boards. Terminal 27 is connected to one side of C4, C3, C13, and C15. Similarly the bus from terminal 33 of board 17 goes to terminal 15 of each board, and terminal 33 of board 18 is connected to terminal 31 (marked YD signal) of each board.

To see how the memory functions, assume that we are just beginning a scan of head 1. (See figure 46.) During the Read time of line 1, the VX1 bus goes high and the VY1 bus goes low. (See waveforms in figure 45A.) The VX1 bus closes switches Q1 through Q4. These switches, connect one side of C1, C4, C5, and C7 on board 15 only, to the I/O bus.

The VY1 bus is connected to the primary of the driver transformer for Q17 on board 15. Consequently at the same time that the VX1 switches close, Q17 on board 15 closes thereby grounding one side of C1, C2, C14 and C16 on each of the four boards, or a total of 16 capacitors. Only one of these 16 capacitors, namely C1 on board 15 is connected to the I/O bus (because Q1 on board 15 is energized by the VX1 bus). Consequently only C1 on board 15 has a complete charge path. Therefore, during the Read time of line 1, in head scan 1, the voltage on C1 of board 15 is applied to the I/O bus.

Since no write period occurs during line 1, the next action occurs during the Read X time of line 2. At this time, the VX2 signal goes high and the VY1 signal again goes low. The VX2 signal causes Q9, Q10, Q11 and Q12 to connect one side of C2, C3, C6, and C8 to the I/O bus. The $\overline{VY1}$ signal returns the same 16 capacitors to ground as in line 1, but of these 16, only C2 on board 15 is connected to the I/O bus. Consequently only the voltage across this capacitor is applied to the I/O bus.

During the Write X time of line 2, once again, VX1 goes high and $\overline{VY1}$ goes low, consequently the charge path of C1 on board 15 is again completed. This time, however, C1, charges to the voltage on the I/O bus, which is the velocity error difference between lines 1 and 2.

In a similar manner (see fig. 47) each of the 16 capacitors grounded by the VY1 signal (C1, C2, C14, C16 on the four boards) is connected to the I/O bus by the corresponding VX signal, during the Read X period of one line and the Write X period of the next, except the capacitor corresponding to VX16 (C16 on board 18). As previously explained the voltage stored on this capacitor serves for both the sixteenth and seventeenth lines (fifteenth and sixteenth on 625-line standards). In a 16 line head scan (15 on 625 line standard) this capacitor is addressed

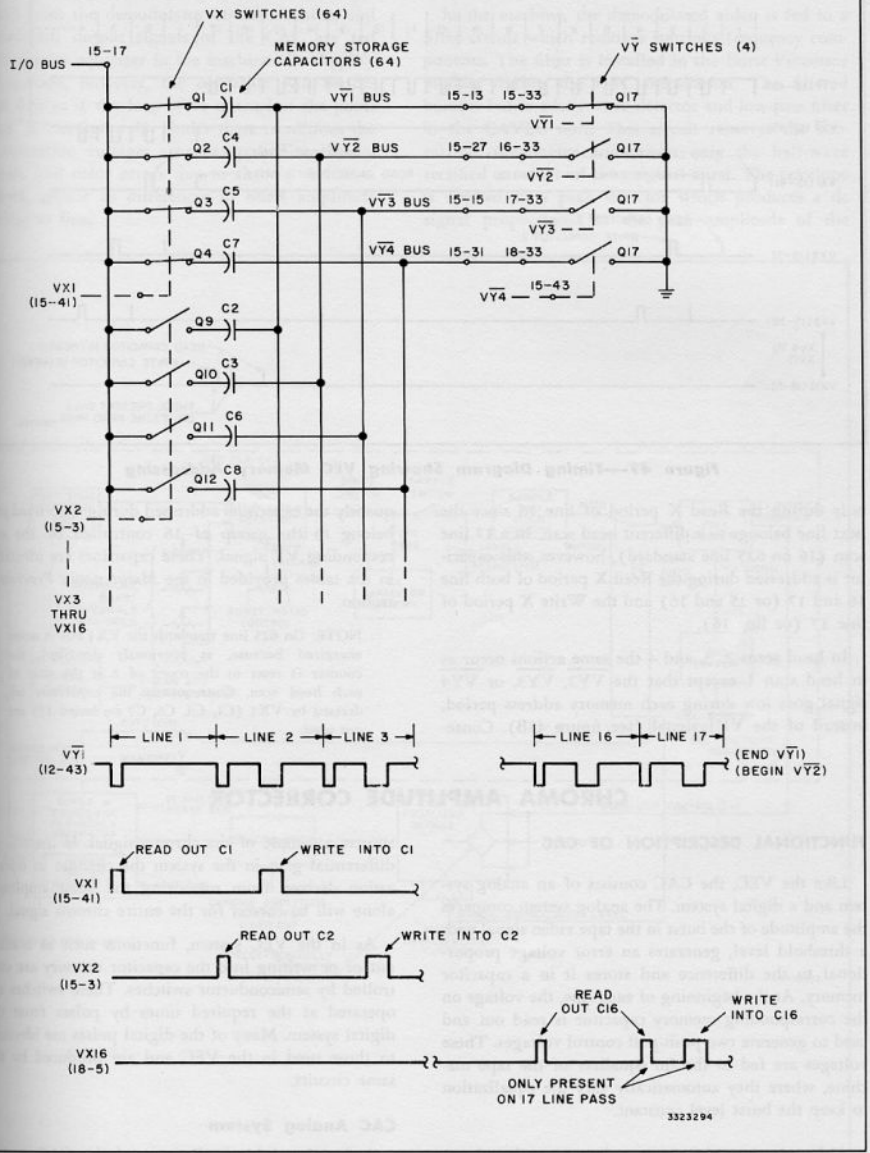


Figure 46—Simplified Diagram of VEC Memory Matrix

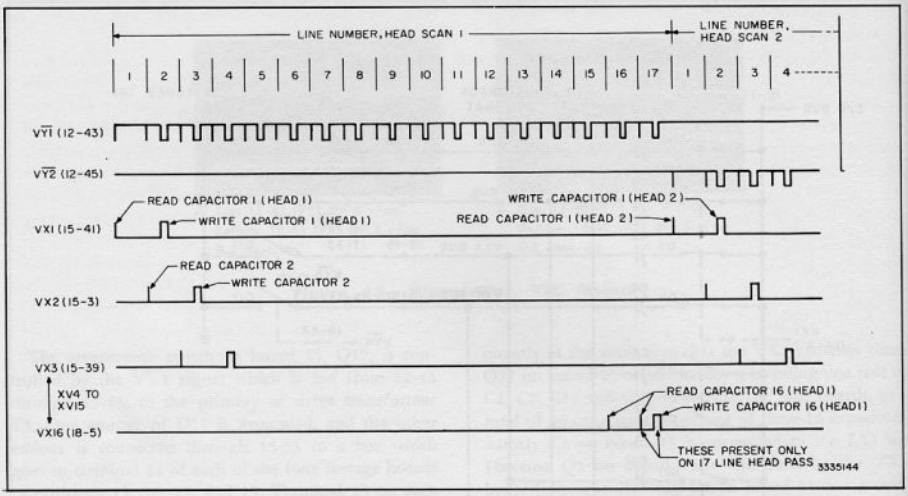


Figure 47—Timing Diagram Showing VEC Memory Addressing

only during the Read X period of line 16 since the next line belongs to a different head scan. In a 17 line scan (16 on 625 line standard), however, this capacitor is addressed during the Read X period of both line 16 and 17 (or 15 and 16) and the Write X period of line 17 (or line 16).

In head scans 2, 3, and 4 the same actions occur as in head scan 1 except that the $\overline{VY2}$, $\overline{VY3}$, or $\overline{VY4}$ signal goes low during each memory address period, instead of the $\overline{VY1}$ signal (see figure 45B). Consequently the capacitors addressed during each head scan belong to the group of 16 controlled by the corresponding $\overline{VY}$ signal. These capacitors are identified in the tables provided in the *Maintenance Procedures* section.

NOTE: On 625 line standards the VX1 bus is never energized because, as previously described, the counter is reset to the count of 2 at the start of each head scan. Consequently the capacitors addressed by VX1 (C1, C4, C6, C7 on board 15) are not used.

CHROMA AMPLITUDE CORRECTOR

FUNCTIONAL DESCRIPTION OF CAC

Like the VEC, the CAC consists of an analog system and a digital system. The analog system compares the amplitude of the burst in the tape video signal with a threshold level, generates an error voltage proportional to the difference and stores it in a capacitor memory. At the beginning of each line, the voltage on the corresponding memory capacitor is read out and used to generate two push-pull control voltages. These voltages are fed to the fm equalizer of the tape machine, where they automatically vary the equalization to keep the burst level constant.

Although the CAC error voltages are based entirely on the burst amplitude, the burst actually constitutes a sample of the chroma signal. If there is no differential gain in the system the changes in equalization derived from measuring the burst amplitude alone will be correct for the entire chroma signal.

As in the VEC system, functions such as reading out of or writing into the capacitor memory are controlled by semiconductor switches. These switches are operated at the required times by pulses from the digital system. Many of the digital pulses are identical to those used in the VEC and are produced by the same circuits.

CAC Analog System

A functional block diagram of the CAC analog system is shown in figure 48. Basic waveforms are

shown in figure 49. Actually the system constitutes a closed loop, since the burst input to the CAVEC is obtained from the demodulator of the machine, and the push-pull output signals of the CAC are fed back to the fm equalizer in the machine. To simplify the discussion, however, the operation will be described first as if the loop were opened at the point marked "X" in figure 48. Under these conditions the CAC correction voltages are not applied to the fm equalizer, and color errors due to chroma variation, therefore, appear as differences in burst amplitude from line to line.

Open Loop Operation

In the machine, the demodulated video is fed to a filter circuit which removes spurious frequency components. The filter is installed in the Burst Processor module during the CAC installation. The filtered burst is fed to a half-wave detector and low-pass filter in the CAVEC unit. This circuit removes the subcarrier components and leaves only the half-wave rectified envelope of the original burst. The envelope is applied to a peak detector which produces a dc signal proportional to the peak amplitude of the

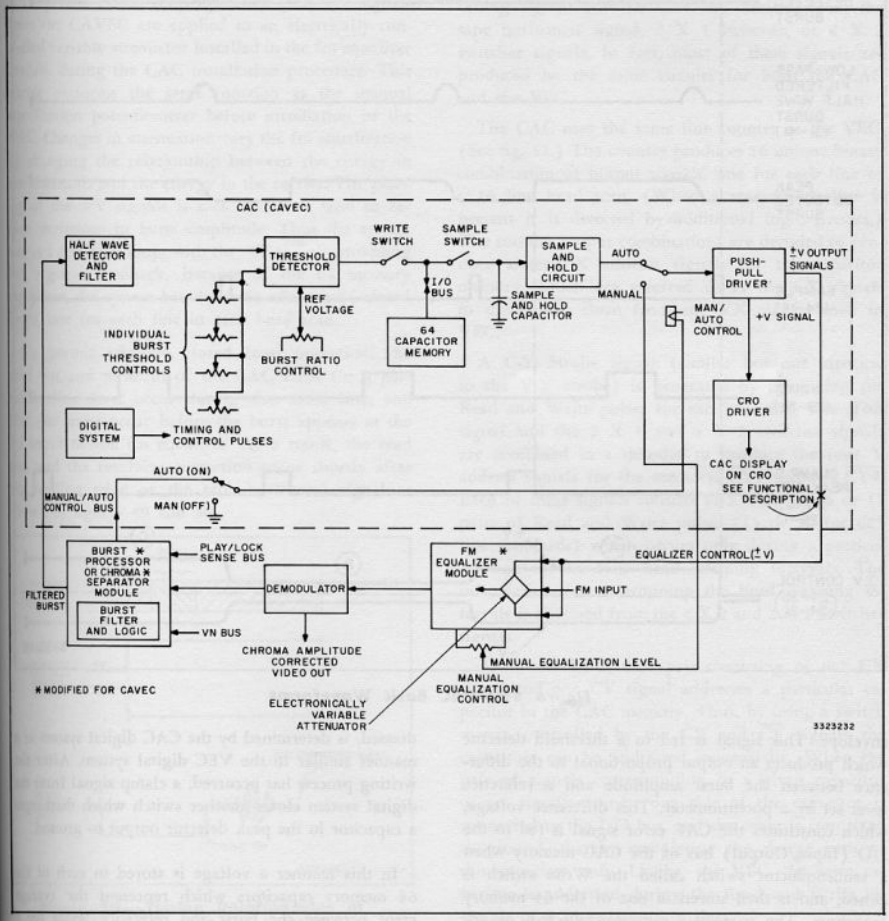


Figure 48—Functional Block Diagram of CAC

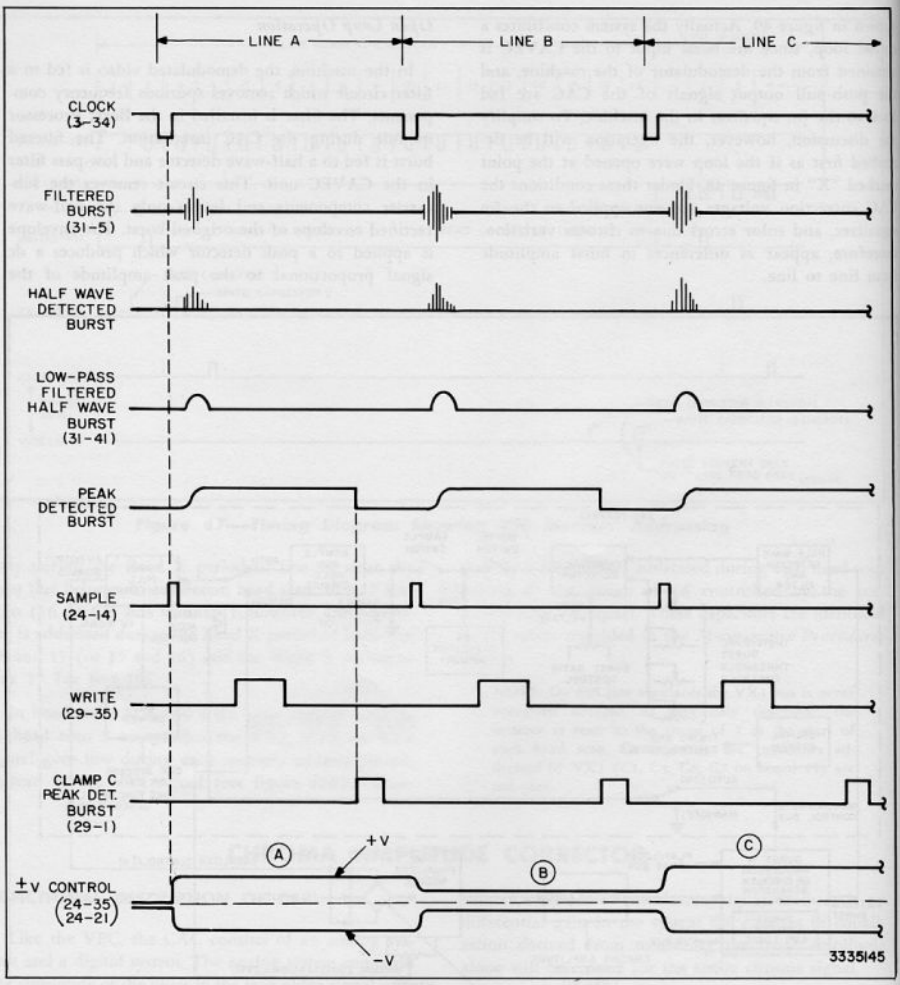


Figure 49—CAC Basic Waveforms

envelope. This signal is fed to a threshold detector which produces an output proportional to the difference between the burst amplitude and a reference level set by a potentiometer. This difference voltage, which constitutes the CAC error signal is fed to the I/O (Input/Output) bus of the CAC memory when a semiconductor switch called the Write switch is closed, and is then stored in one of the 64 memory capacitors. The particular capacitor selected, or addressed, is determined by the CAC digital system in a manner similar to the VEC digital system. After the writing process has occurred, a clamp signal from the digital system closes another switch which discharges a capacitor in the peak detector output to ground.

In this manner a voltage is stored in each of the 64 memory capacitors which represent the average error between the burst and reference levels for a

particular line in a particular head scan interval. At the start of each line, the CAC error signal stored in the corresponding capacitor is read out by applying it to the I/O bus. During the Read interval, a switch transfers the voltage from the I/O bus to a capacitor in the sample and hold amplifier, which serves as a temporary memory. The output of the sample and hold amplifier is fed to two drivers which develop push-pull control voltages (± V) proportional to the sampled error. These two signals constitute the CAC control output of the CAVEC unit.

Closed Loop Operation

To permit closed loop operation, the ±V signals from the CAVEC are applied to an electrically controlled variable attenuator installed in the fm equalizer module during the CAC installation procedure. This circuit performs the same function as the manual equalization potentiometer before installation of the CAC. Changes in attenuation vary the fm equalization by changing the relationship between the energy in the sidebands and the energy in the carrier. The phasing of the ±V signals is such that they tend to reduce variations in burst amplitude. Thus the system acts as a feedback loop, with the ±V signals providing the negative feedback. Because of the 64 memory capacitors, the system has the same effect as 64 closed loops, one for each line in each head scan.

To permit effective closed loop operation, the read out and write in of the CAC error for a particular line must occur during that same line, and read out must occur before the burst appears at the fm input of the fm equalizer. As a result, the read out, and the resulting correction occur shortly after the leading edge of the tape horizontal signal as shown in figures 49 and 50.

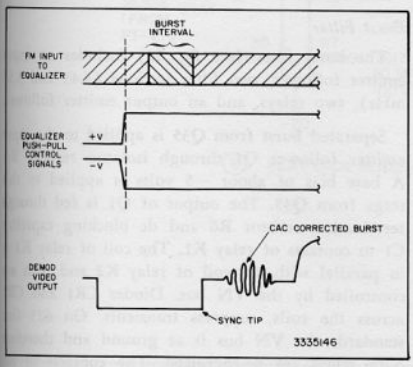


Figure 50—Timing Relationships of Burst in FM to Burst in Video

For a seventeen line head pass, on 525 line standards, the error voltage on the capacitor written into during the sixteenth line is read out during both the sixteenth and seventeenth line. (Similarly, on 625 line standards, the capacitor written into during the fifteenth line is read out during both the fifteenth and sixteenth lines). The inaccuracy thus produced, is not visible in the picture because a seventeenth line does not occur periodically during successive scanning periods of the same video head.

CAC Digital System

As in the VEC, previously described, the basic timing signals for the CAC are derived from the tape horizontal signal, 2 X 1 switcher, or 4 X 2 switcher signals. In fact, most of these signals are produced by the same circuits for both the CAC and the VEC.

The CAC uses the same line counter as the VEC. (See fig. 51.) The counter produces 16 unique binary combination of output signals, one for each line of a 16 line head scan. (When a seventeenth line is present it is detected by additional logic circuits.) The counter output combinations are decoded to produce sixteen X address signals for the capacitor memory, which are referred to as the CX signals to distinguish them from the VX signals used in VEC.

A C-Y Strobe signal (similar but not identical to the V-Y strobe) is generated by combining the Read and Write pulses for each scanning line. This signal and the 2 X 1 and 4 X 2 switcher signals are combined in a decoder to produce the four Y address signals for the memory, $\overline{CY1}$ through $\overline{CY4}$. Each of these signals consists of a train of 16 or 17 pairs of Read and Write pulses (15 or 16 for 625 line standards) which occurs only during a particular one of the four head scanning intervals. The information for determining the head scanning intervals is obtained from the 4 X 2 and 2 X 1 Switcher signals.

As in the VEC, each pair consisting of one CX signal and one CY signal addresses a particular capacitor in the CAC memory. Thus, by using a switch matrix controlled by the CX and $\overline{CY}$ signals the capacitors can be addressed sequentially. When the pair of signals corresponding to a given capacitor occurs simultaneously, one side of the capacitor is connected to the I/O bus, and the other is connected to ground, thereby completing the charge path of this capacitor only. Unlike, the VEC, the same capacitor is addressed during the Read and Write intervals of a given scanning line.

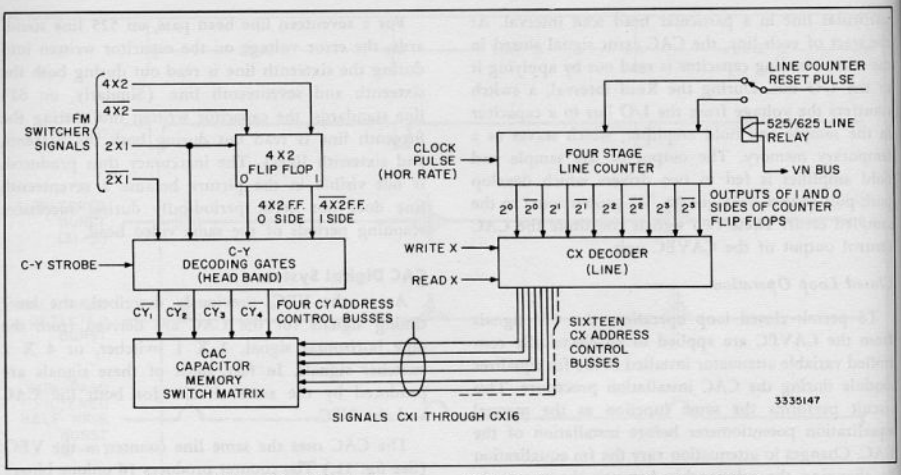


Figure 51—Simplified Diagram of CAC Memory Control Circuits

DETAILED DESCRIPTIONS OF CAC ANALOG SYSTEM

The CAC circuits in the Burst Processor Module, FM Equalizer module, and the analog boards in positions 31, 29, 24, and 23, of the CAVEC module are described in detail in the following paragraphs.

The order of the descriptions generally follows that of section 7 of the logic diagram (figure 111). This diagram should be referred to for interconnections between the various boards. The schematic diagram of the individual board should be referred to for internal circuit details.

Burst Filter Board (Module 632 in TR-70 or Y17 in TR-60)

The burst filter board (see fig. 52) is added to the Burst Processor Module during the CAC installation. The board includes a burst filter and the PLAY/LOCK SENSE/BURST SENSE (PLAY/L.S./B.S.) logic circuit.

The burst filter is a high quality band pass filter designed to remove spurious frequency components from the burst before it is fed to the CAVEC. The filter has separate sections for use on 525 line standards (3.58 mHz subcarrier) or 625 line standards (4.43 mHz subcarrier). The required section is automatically selected by relays controlled by the VN bus.

The PLAY/L.S./B.S. logic circuit provides a control signal to the AUTO/MANUAL relay on the Push-Pull Driver, Board 24, of the CAVEC which allows the CAC to enter the AUTOMATIC mode only when the machine is in PLAY, a Lock condition is achieved and the presence of burst is sensed. These conditions are desirable for automatic equalization because of the following:

1. Unless the machine is in PLAY, the video in the playback system can be obtained only from E-E (electronic-to-electronic) operation, and therefore, no errors will be present for the CAC to correct.

2. Before the LOCK condition is achieved, the CAC memory will not be stabilized enough for reliable CAC operation.

3. If burst is not present the CAC has no basis for determining automatic equalization.

Burst Filter

The burst filter (see fig. 52) includes an input emitter follower, two filter sections (4.43 and 3.58 mHz), two relays, and an output emitter follower.

Separated burst from Q35 is applied to the input emitter follower Q1 through isolaton resistor R4. A base bias of about −5 volts is applied to this stage from Q35. The output of Q1 is fed through termination resistor R6 and dc blocking capacitor C1 to contacts of relay K1. The coil of relay K1 is in parallel with the coil of relay K2 and both are controlled by the VN bus. Diodes CR1 and CR2 across the coils, suppress transients. On 625 line standards the VN bus is at ground and therefore both relays are de-energized. The contacts of K1 then feed the signal from C1 into the 4.43 mHz

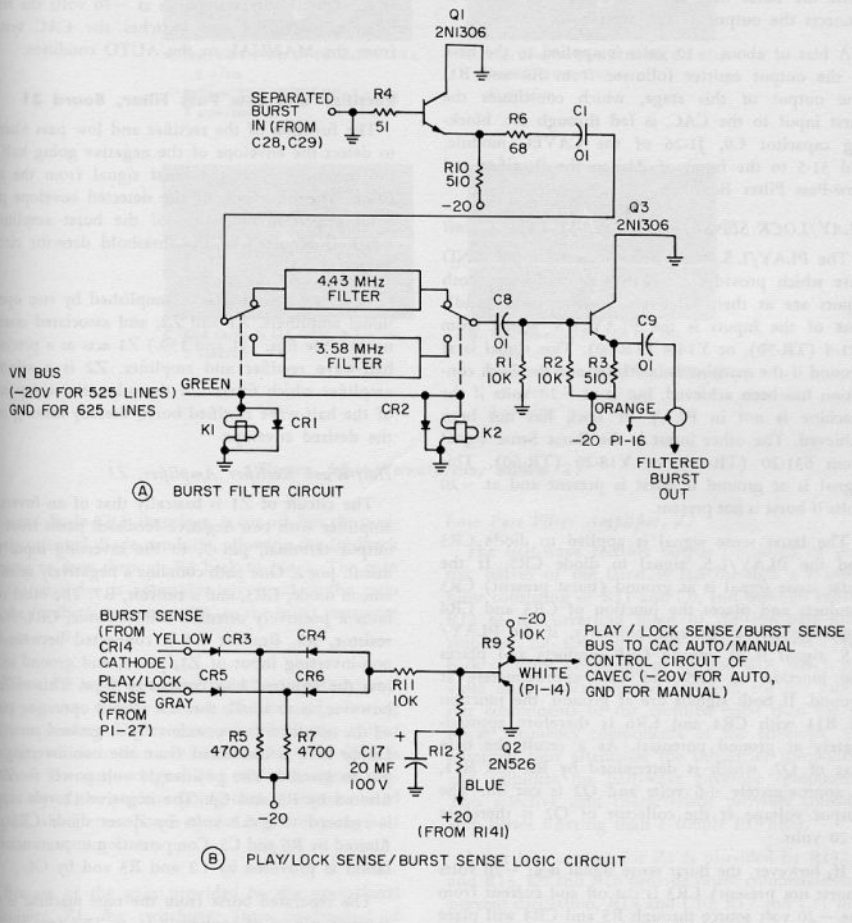


Figure 52—Partial Schematic Diagram Showing Burst Filter and PLAY/L.S./B.S. Logic Circuit Board

filter section, and the contacts of K2 feed the output of this filter section through dc blocking capacitor C8 to the output emitter follower Q3.

On 525 line standards the VN bus is at −20 volts and, therefore both relays are energized. K1 then feeds the burst into the 3.58 mHz filter and K2 connects the output of this section to C8.

A bias of about −10 volts is applied to the base of the output emitter follower from R2 and R1. The output of this stage, which constitutes the burst input to the CAC, is fed through d.c. blocking capacitor C9, J1-26 of the CAVEC module, and 31-5 to the input of Z1, on the Rectifier and Low-Pass Filter Board.

PLAY/LOCK SENSE/BURST SENSE Logic Circuit

The PLAY/L.S./B.S. circuit is a two-input AND gate which provides a negative output when both inputs are at their relatively positive level (gnd). One of the inputs is the PLAY/L.S. signal from 621-4 (TR-70), or Y14-4 (TR-60). This signal is at ground if the machine is in PLAY and the Lock condition has been achieved, but is at −20 volts if the machine is not in PLAY or Lock has not been achieved. The other input is the Burst Sense signal from 631-20 (TR-70), or Y18-20 (TR-60). This signal is at ground if burst is present and at −20 volts if burst is not present.

The burst sense signal is applied to diode CR3 and the PLAY/L.S. signal to diode CR5. If the burst sense signal is at ground (burst present) CR3 conducts and places the junction of CR3 and CR4 approximately at ground. Similarly, if the PLAY/L.S. signal is at ground CR5 conducts and places the junction of CR5 and CR6 approximately at ground. If both signals are at ground, the junction of R11 with CR4 and CR6 is therefore approximately at ground potential. As a result the base bias of Q2, which is determined by R8 and R11, is approximately +6 volts and Q2 is cut off. The output voltage at the collector of Q2 is therefore −20 volts.

If, however, the burst sense signal is at −20 volts (burst not present) CR3 is cut off and current from the −20 volt source through R5 and CR4 will place the junction of R11 with CR4 and CR6 at approximately −12 volts. Q2, therefore is forward biased and its collector voltage goes to ground. Similarly, if the PLAY/L.S. signal is at −20 volts, CR5 is cut off, Q2 conducts and its collector goes to ground.

The collector voltage of Q2 which constitutes the PLAY/L.S./B.S. or CAC AUTO/MAN control signal is fed through J1-15 of the CAVEC Module to the CAC AUTO/MANUAL switch, S2, on the front panel. If this switch is in the ON Position it connects the PLAY/L.S./B.S. signal to a relay driver circuit on Board 23. This circuit drives the Manual/Auto relay K1 on the Push-Pull Driver, Board 24. If the CAC Control signal is at −20 volts the relay becomes energized and switches the CAC system from the MANUAL to the AUTO condition.

Rectifier and Low Pass Filter, Board 31

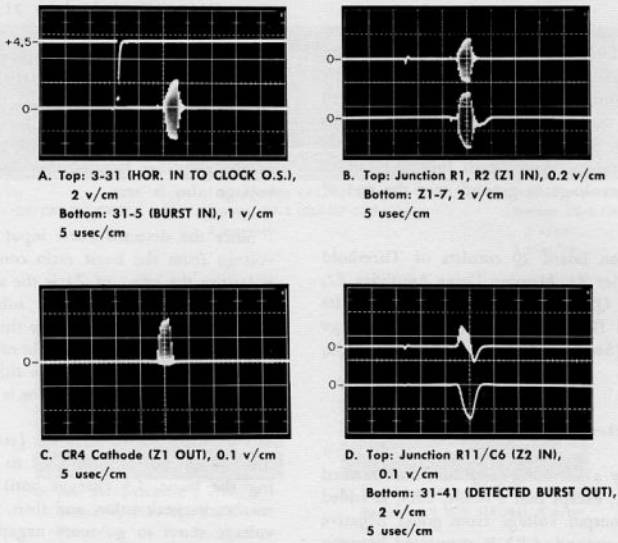
The function of the rectifier and low pass filter is to detect the envelope of the negative going half of the incoming separated burst signal from the machine. The waveform of the detected envelope provides a precise indication of the burst amplitude, which is required by the threshold detector circuit on board 29.

Envelope detection is accomplished by two operational amplifiers, Z1 and Z2, and associated components. (See figs. 111 and 139.) Z1 acts as a precision half-wave rectifier and amplifier. Z2 is a selective amplifier which filters out the subcarrier component of the half-wave rectified burst, thereby leaving only the desired envelope.

Half-Wave Rectifier Amplifier, Z1

The circuit of Z1 is basically that of an inverting amplifier with two negative feedback paths from the output terminal, pin 7, to the inverting input terminal, pin 2. One path contains a negatively oriented silicon diode, CR3, and a resistor, R7. The other contains a positively oriented silicon diode, CR4, and a resistor, R8. Resistor R4 is connected between the non-inverting input of Z1, pin 3, and ground to allow the required bias current to flow. This current, however, is so small, that the output operating point of the amplifier is approximately at ground potential. Diode CR1 is connected from the non-inverting input to ground. The positive 12-volt power for Z1 is filtered by R5 and C3. The negative 12 volt supply is reduced to −6.2 volts by Zener diode CR5 and filtered by R6 and C5. Compensation to prevent oscillation is provided by C2 and R3 and by C4.

The seperated burst from the tape machine is fed through pin 26 of connector J1, to 31-5 (see fig. 111 and waveforms in fig. 53A). The burst is then fed through coupling capacitor C1, and voltage divider R19 and R1, which attenuates the signal, to the input resistor, R2, of Z1. When the burst applied to R2 goes negative (below ground), the output at terminal 7 goes positive, because the input signal is applied to the inverting input. (See fig. 53B.) The negatively



A. Top: 3-31 (HOR. IN TO CLOCK O.S.), 2 v/cm
Bottom: 31-5 (BURST IN), 1 v/cm
5 usec/cm

B. Top: Junction R1, R2 (Z1 IN), 0.2 v/cm
Bottom: Z1-7, 2 v/cm
5 usec/cm

C. CR4 Cathode (Z1 OUT), 0.1 v/cm
5 usec/cm

D. Top: Junction R11/C6 (Z2 IN), 0.1 v/cm
Bottom: 31-41 (DETECTED BURST OUT), 2 v/cm
5 usec/cm

Figure 53—Waveforms, Board 31

oriented diode CR3, therefore, is cut off, but the positively oriented diode conducts, allowing the feedback current to flow through R8 back to pin 2. The gain of the amplifier is approximately equal to the ratio of the feedback resistance, R8, to the input resistance R2, or −10.

When the input goes positive, the output at pin 7 goes negative, thereby cutting off CR4 and allowing CR3 to conduct. Under these conditions, the output voltage, which is taken from the cathode of CR4, is ground. The output signal (fig. 53C) therefore consists only of the positive going half of the amplified signal, which corresponds to the negative going half of the incoming burst.

Because of the gain provided by the operational amplifier, Z1, the switchover from conduction of CR4 to CR3 occurs almost exactly when the input voltage crosses its ac axis, thereby providing precision half-wave rectification. If an operational amplifier were not used, switchover could not occur until the incoming burst was either above or below its axis by an amount equal to the threshold voltage of the silicon diodes. This would create problems at low signal levels.

Low Pass Filter Amplifier, Z2

The half-wave rectifier output consisting of positive halves of the burst is fed through a low-pass filter consisting of R11 and C6, and through resistor R12 to the inverting input of the low-pass filter-amplifier, Z2. (See fig. 53D.) This circuit has a feedback network, consisting of C7 and R18, which provides much more negative feedback for the subcarrier components of the rectified burst than for the lower frequency components of the envelope. The amplifier thus attenuates the subcarrier components and amplifies the half-wave envelope components. This selective gain characteristic provides considerably better filtering than a simple RC filter.

Input bias current for Z2 is provided by R15. C8 and R13, C9 and R16 provide phase compensation to prevent oscillation. R14 and C10, R17 and C11 filter the power supply voltages.

Z2 inverts the input signal in addition to filtering it. The output of Z2 (fig. 53D, bottom waveform) therefore consists of a negative going signal which follows the outline of the positive going peaks in the input signal, but contains no subcarrier components. This signal is fed through 31-41 and 29-7, to one input of the threshold detector on board 29.

Threshold Detector, Board 29

The functions of the threshold detector (see section 7 of Logic Diagram, fig. 111) are (1) to obtain an error voltage proportional to the amount by which the amplitude of the detected burst from board 31 exceeds a dc threshold voltage, (2) to apply this error voltage to the I/O bus of the CAC memory during the Write portion of each line and (3) to clamp the error voltage to ground near the end of each line.

The circuits on board 29 consists of Threshold Detector Amplifier Z1, Memory Drive Amplifier Z2, Clamp C Switch Q1, Write Switch Driver Q3, Write Switch Q2, and Burst Ratio potentiometer voltage regulator CR1. (See Schematic Diagram of Board 29, figure 137.)

Threshold Detector Amplifier, Z1

Z1 is basically a summing amplifier, as described in the *Appendix*, except that a diode, CR3, is added to prevent the output voltage from going negative with respect to ground. CR2 is connected between the output terminal, pin 9 of Z1, and the feedback resistor, R26. CR3 is connected from the output terminal to the inverting input, pin 2.

The input voltages are applied through two 21.5K resistors, R3, R4 to the inverting input, pin 2, of Z1. Resistor R5, connected between the non-inverting input, pin 3 of Z1, and ground, allows a small amount of input bias current to flow. The networks consisting of C1, C10 and R6, and R7 and C3, prevent oscillation, R8, C2, and R9, C4, filter the power supply voltages.

The detected burst from 31-41 is fed through 29-7 to input resistor R3. A dc voltage from the BURST RATIO potentiometer on the CAVEC front panel. is fed through 29-5, to the second input resistor, R4.

The burst input to R3 is negative, and the BURST RATIO control voltage applied to R4 is positive. When the sum of the voltages applied to the input resistors is negative, the output voltage tends to be positive, because the amplifier is of the inverting type. CR2, therefore, conducts placing R26 in the feedback loop, and CR3 is cut off. The circuit then behaves as a normal summing amplifier. Since the input resistors, R3, and R4 are equal (21.5K ohms) the output voltage is equal to the sum of the input voltages applied to the resistors multiplied by a gain factor of about 3.5 (the value of feedback resistor R26, 75K, divided by 21.5K).

Conversely, when the sum of the input voltages is positive, the output tends to be negative. CR2 then opens and disconnects R26, while CR3 conducts and short circuits the output terminal to the inverting input terminal. Under these conditions, the gain of the amplifier is effectively zero, and the output voltage also is zero.

Since the detected burst input and the threshold voltage from the burst ratio control have opposite polarities the effect of Z1 is the same as if they had the same polarity and were subtracted from each other. If the burst exceeds the threshold Z1 tends to amplify the difference by a gain of −3.5. If, however, the burst does not exceed the threshold, the gain is zero, and the output, therefore is at ground level.

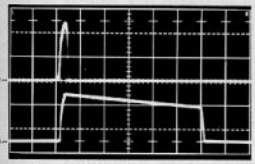
The output of the amplifier (see waveforms in figure 54A) is fed through CR2 to capacitor C5. During the burst, C5 charges until the error voltage reaches its peak value, and then, when the amplifier voltage starts to go more negative than this peak value, the voltage on C5 reverse biases CR2. Since the time constant of C5 and R26 is large, C5 therefore essentially remains charged to the peak voltage until the arrival of the Clamp C pulse, described later. The peak positive voltage is fed through R10 to the non-inverting input of the CAC Memory Drive Amplifier Z2.

Clamp C Switch

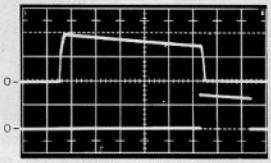
The Clamp C switch circuit, consisting of Q1, T1, R18 and R19 is provided to remove the charge from C5 near the end of each line. This allows the capacitor to charge to a completely new voltage during the next burst. The output of the Clamp C driver on the Timing B board is fed through 2-5 and 29-1 to R19, which is in series with the primary of T1. As explained under *CAC Digital System* the Clamp C signal goes high for a period of 10 microseconds near the end of each line. During this period Q1 conducts, thereby shorting C5 to ground and completely discharging it. (See fig. 54B.)

CAC Memory Driver Amplifier, Z2

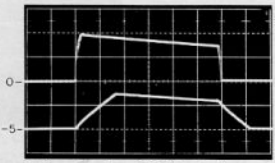
Z2 is an operational amplifier of the differential input type as described in the *Appendix*. The peak error signal from C5 is applied through R10 to the non-inverting input. +6 volts dc from a voltage di-



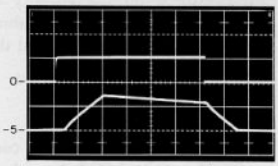
A. Top: Z1-9, 2 v/cm
Bottom: Junction C5/CR2 (Z1 OUT), 2 v/cm



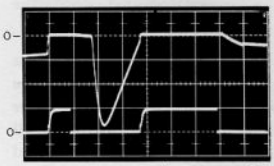
B. Top: Junction CR2/C5, 2 v/cm
Bottom: 29-1 (CLAMP C) 2 v/cm
5 usec/cm



C. Top: Junction CR2/C5, 2 v/cm
Bottom: Z2-6 (MEMORY DRIVE OUT) 5 v/cm
5 usec/cm



D. Top: 29-35 (WRITE), 2 v/cm
Bottom: Junction CR2/C5, 5 v/cm
5 usec/cm



E. Top: 29-45 (CAC I/O BUS), 1 v/cm
Bottom: 5-9 (C-Y STROBE), 5 v/cm
5 usec/cm

Figure 54—Waveforms, Board 29

vider consisting of R11, R12, and R13 is applied to the inverting input. Feedback from the output to the inverting input is applied through R14. R15, C6 and C8 prevent oscillation. R16, C7, R17, and C9 provide power supply filtering.

As explained in the *Appendix,* the gain of Z2 for the two input voltages is determined by the feedback resistor, R14, and the input resistor, R13. Since these two resistors are equal, the gain for the +6 volts dc applied to R13 is −1, while the gain for the error signal applied to R10 is +2. The output voltage (fig. 54C, bottom waveform) therefore is the sum of two components, one equal to −6 volts, and the other equal to twice the error input voltage.

This output voltage will normally be near ground potential. Consequently, the component due to the error voltage must be approximately +6 volts, to make the sum zero. This means that the signal input from Z1 must be approximately +3 volts. To produce the +3 volts, a sufficiently large difference must exist between the detected burst and the reference voltages at the input to the threshold amplifier Z1. This difference is maintained constant by the automatic adjustment of the burst amplitude produced by the fm equalizer. (A small net error voltage, however, will always be present at the output of Z2 to permit generating the push-pull control signal required by the fm equalizer.)

CAC Write Switch

The output of Z2 which constitutes the CAC error signal, is fed to one emitter of Write switch Q2. The other emitter of Q2 is connected through R20, 29-45, and 25-17 to the I/O bus of the CAC memory. Q2 is controlled by the Write signal from 4-9 which is applied through 29-35 and R22 to the base of transformer driver Q3. (See fig. 54D.) The Write signal is normally low (0 volts) and consequently Q3 is cut off by positive bias from the +4.5 volt source applied through R24 and CR4 to its emitter. During the Write period of each line, however, the Write signal goes high, thereby forward biasing Q3. Current from Q3 then energizes T2 causing Q2 to conduct and feed the output of Z2 to the I/O bus. (See fig. 54E.)

Power Supply for BURST RATIO Control

The circuit consisting of R1, Zener diode CR1, and R2 provides voltage for the BURST RATIO control on the CAVEC front panel. R2 is connected through 29-19 to one end of the BURST RATIO potentiometer. CR1 reduces the +12 volts applied to R2 to ap-

proximately 6.2 volts. Since the potentiometer has a value of 500 ohms and R2 has a value of 511 ohms, the voltage applied to the control is approximately +3 volts.

Push-Pull Driver, Board 24

The Push-Pull Driver, Board 24, performs the following functions:

1. When CAC is in AUTO condition, samples the output voltage of the capacitor memory once per line, transfers it to a holding capacitor and develops two pushpull dc output voltages proportional to the sampled voltage. These two voltages, which constitute the output signals of the CAC control the automatic equalizer in the fm equalizer module of the machine.

2. When CAC is in MANUAL, disconnects the sample and hold circuits and substitutes a dc voltage from the equalizer potentiometer or the fm equalizer module, for the sample voltage. The two push-pull output signals are then proportional to the manual equalization voltage instead of the sample voltage.

The circuits on board 24 (see schematic diagram, figure 133), includes three operational amplifiers, Z1, Z2, Z3 a semiconductor switch, Q1, and a relay K1. Z1 is the memory read amplifier, Z2, the first push-pull output stage, and Z3, the second push-pull output stage. Q1 connects the output of Z1 to a holding capacitor in the input circuit of Z2 during the sample period of each line. K1 switches the circuit either to automatic or manual operation.

CAC Memory Read Amplifier, Z1

The function of Z1 is to provide isolation between the I/O bus of the CAC Memory and the Sample and Hold circuit. Z1 is connected as a voltage follower and therefore has a gain of +1. Feedback to the inverting input is provided through R2. Diodes CR1, CR2 and CR8, between the non-inverting input and ground, limit both the positive and negative excursions of the input signal to prevent saturating the amplifier. C1, C4 and R5 prevent oscillation. R3, C2, R4, and C3 provide power supply filtering.

The I/O bus of the CAC capacitor memory is connected from 25-17, through 24-7, to the input resistor, R1, of Z1. Contact K1A-3 of the MANUAL/AUTO relay is also connected to R1. In the MANUAL or OFF condition, K1 is de-energized, and K1A grounds the input of Z1. In the AUTO condition, K1 is energized, and K1A ungrounds the input of Z1 allowing the voltage on the I/O bus to enter the amplifier.

Sample and Hold Circuit, Q1, R7, C5

The output of Z1 is fed to one emitter of switch Q1. The other emitter is connected through surge current limiting resistor R7 to the sample and hold capacitor, C5. Q1 is controlled by the $\overline{\text{Sample CAC}}$ signal from 5-25 which is fed through 24-14 to the primary of drive transformer T1. During the sample period of each line the $\overline{\text{Sample CAC}}$ signal goes low causing Q1 to conduct. (See waveforms in figure 55A). C5 then charges to the voltage stored in the memory capacitor connected to the I/O bus. This memory capacitor is the one addressed during the Read interval since the sample period occurs within this interval. After C5 charges to the level of the voltage stored on the memory capacitor, it holds this correction voltage for the duration of the entire line. For this reason, it is called the sample and hold capacitor.

First Push-Pull Amplifier, Z2

If the CAC is in the AUTO condition the voltage on C5 (fig. 55B) is fed through relay contacts K1B to the non-inverting input of the first push-pull output amplifier, Z2. If the CAC is in MANUAL, however, K1B disconnects C5 and applies the Manual Equalization voltage from 24-43 to the non-inverting input of Z2.

Z2 is connected as a non-inverting amplifier, with a gain characteristic modified by the action of a diode, CR3, connected across the feedback resistor, R11. C7, R10, C14 and R13, prevent oscillation. R14, C10, R12, and C8 provide power supply filtering.

When the input voltage is negative the output voltage is also negative and CR3, therefore, is reverse biased. Under these conditions, the gain of the amplifier, determines by R11 and R30, is approximately +10. When, however the input is positive, CR3 is forward biased thereby, shorting out R11. Under these conditions the gain is zero and the output is therefore at ground.

The output of Z2 (fig. 55C, bottom waveform) is fed to a clamp circuit consisting of R15, R16, R17, CR4, CR5, and CR6. This clamp circuit prevents the voltage from going more positive than about −0.7 volts. The output of Z2 (fig. 55D, bottom) constitutes the −V output signal of the CAC. This signal is fed through 24-21 to the CAC −test point, TP4 on the front panel of the CAVEC and through J1-21 to the (−) input of the attenuator board on the fm equalizer module of the machine. The −V signal is also fed through R22 to the inverting input of Z3.

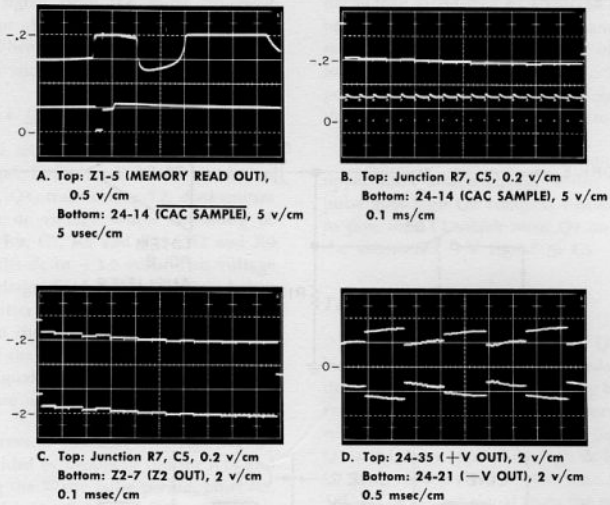


Figure 55—Waveforms, Board 24

Second Push-Pull Output Amplifier, Z3

Z3 is connected as a unity gain inverting amplifier, and therefore provides an output voltage equal and opposite to that of Z2. This output, which is called the +V signal, (fig. 55D, top) is fed through 24-35 and J1-20 to the (+) input of the attenuator board on the fm equalizer module. The signal is also fed through 23-24 to the display clamp switch on the CRO Relay Driver board for display purposes on the CRO.

To insure that the +V output is balanced with respect to the −V output from a dc as well as an ac standpoint, a balance control circuit consisting of fixed resistors R18 and R20, and potentiometer R19 is provided in the inverting input circuit of Z3. The range of the balance control potentiometer, R19, is determined by R18 and R20. The output voltage of the balance control is filtered by C11.

R26 provides a small amount of input current to Z3 which is required for bias. C12, R23, C14, and R27 prevent oscillation. R25, C13, R28, and C15 provide power supply filtering.

MANUAL/AUTO Relay, K1

One side of the coil of relay K1 is connected through 24-41 and J1-11 to −26 volts dc. The other side is connected through 24-42 and 23-39 to the output of the relay driver on board 23. (See fig. 57.) When the CAC selector switch on the front panel is in the AUTO (ON) position, and the Play/Lock Sense/Burst Sense bus from the Burst Processor Module or Chroma Separator Module is energized, (−20 volts) the relay driver output is grounded and K1 is therefore energized. K1A and K1B then place the circuits in the AUTO condition as previously described. R29, C16 and CR7 suppress transients in the coil circuit of K1.

CRO/Relay Driver, Board 23

The CRO/Relay driver produces the CAC error display signal for the CRO, and provides the drive signal for the MANUAL/AUTO relay, K1, on the Push-Pull Driver, Board 24.

The principal components of the CAC error display circuit consists of the CAC Display clamp switch, Q1, Upper Limit Switch, Q3, and totem pole amplifier Q5, Q6 (*See Simplified diagram of CAC CRO Display Circuit*, figure 56). One side of each switch is connected to the junction of the input capacitor C1, and resistor R10. Q1 is controlled by the Clamp CAC pulse from the digital system and Q3, by the Write Pulse. The timing of these pulses for the first three lines of a head scan is shown in the lower half of

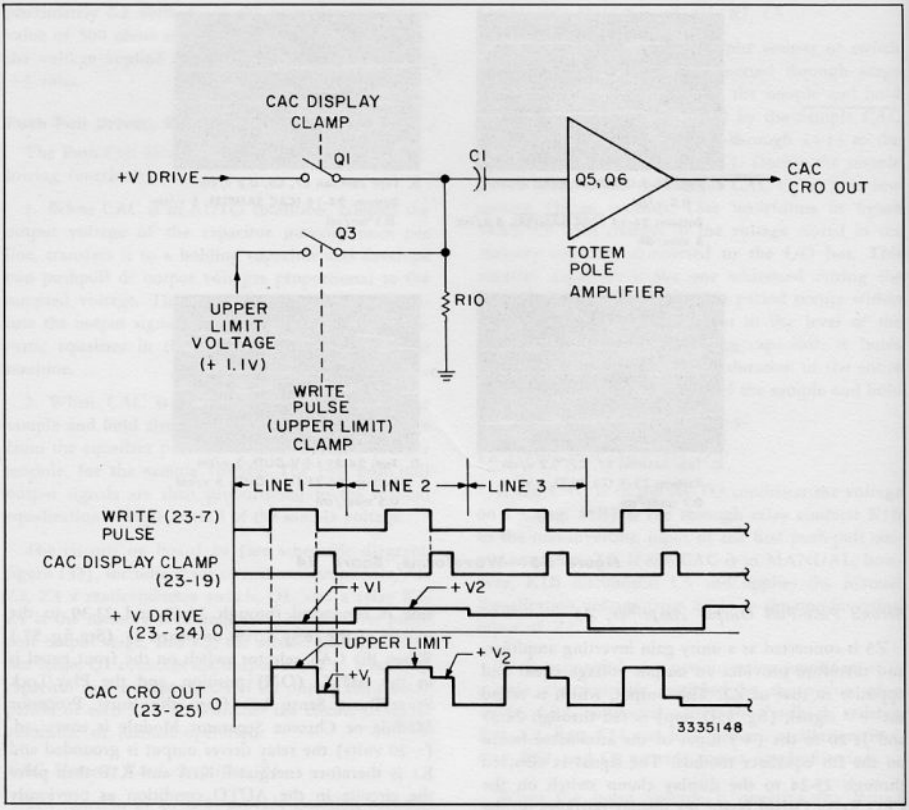


Figure 56—Simplified Diagram of CAC CRO Display Circuit

figure 56. At the start of a line (for example line 1) both pulse signals are low, and the two switches, therefore, are open. Under these conditions, since C1 is returned to ground through R10, the input voltage to C1 is ground. When the Write pulse occurs Q3 closes and feeds +1.1 volts dc from a regulator circuit to C1.

When the CAC Display Clamp pulse occurs, Q1 closes and feeds a signal derived by attenuating the +V signal from the Push-Pull Driver Board, to C1. The input to C1, therefore assumes three different levels in each line: ground, the attenuated +V signal, and +1.1 volt upper limit. The output voltage of Q5 and Q6 assumes corresponding levels. Because the switching occurs rapidly each level appears on the CRO as a continuous horizontal line. The lowest line, corresponds to ground at the input of C1. The middle line represents the +V signal itself. The upper line, which corresponds to the +1.1 volt input to C1, represents the highest value that the +V signal can assume and still be within the correction range of CAC. The display thus permits observing whether the CAC is functioning normally. (In the Manual mode, the +V line is normally approximately midway between the two limits.)

The Relay Driver Circuit consists of a single stage, Q7. As shown in figure 57. Q7 is controlled by the CAC AUTO/MANUAL switch on the CAVEC front panel. When the switch is in the MANUAL position it grounds the input to Q7, thereby cutting it off and de-energizing the relay. In the AUTO position, the switch connects the PLAY/

L.S./B.S. control signal from the Burst Processor module to the input of Q7. If this bus is at ground, Q7 remains off. When, however, the bus is at −20 volts Q7 conducts and energizes the relay.

Upper Limit Switch Q3

As shown in the schematic diagram of board 23, figure 131, the upper limit switch circuit consists of transformer driver, Q4, transformer T2, dual-emitter switch, Q3, and a dc voltage source consisting of Zener diode CR2, R9, C2, R8 and R7. CR2 and R9 reduce the +12 volts dc to +3.9 volts. This voltage is attenuated by voltage divider R7 and R8 and then applied to one emitter of Q3. The other emitter of Q3 is connected to the junction of R10 and C1 in the input circuit of the totem-pole amplifier, Q5, Q6. The Write drive signal from 4-9 is fed through 23-7 and R16 to the base of Q4. (See fig. 58A.)

Normally Q4 is reverse biased by a voltage slightly above ground provided by dropping resistor R18 and diode CR4. During the Write pulse period, however, the base goes positive and causes Q4 to conduct. Current then flows into the primary of T2, thereby turning Q3 on. Q3 then applies the voltage at the junction of R7 and R8 to C1, thereby raising the voltage applied to C1 from ground to approximate +1.1 volts.

+V Switch, Q1

The CAC display switch circuit consists of transformer driver Q2, transformer T1, and dual emitter switch Q1. The +V signal from the push-pull driver on board 24 is fed through 24-35 to 23-24. The signal is then attenuated by a voltage divider consisting of R1 and R3, filtered by C8, and applied to one emitter of Q1. The other emitter of Q1 is connected to the junction of R10 and C1. The CAC display pulse (fig. 58B) from the Timing B board is fed through 2-41, to 23-19, and R5 to the base of Q2.

This circuit functions in the same manner as the upper limit switch circuit. When the CAC display pulse goes high Q2 conducts thereby causing current to flow into T1 which turns Q1 on. Q1 then applies the attenuated +V signal to C1.

Totem Pole Amplifier, Q5, Q6

The totem-pole amplifier Q5, Q6 has unity gain but provides a low output impedance required for driving the CRO. The circuit may be described as an emitter follower, in which Q6 serves as a dynamic emitter resistance for Q5. The input signals from Q1 and Q3 are applied through dc blocking capacitor C1 and resistor R14 to the base of Q5. (See fig. 58C.) The output signal from the emitter of Q6 (fig. 58E), is fed through C5 and 23-25 to the CAC error test point, TP3, on the CAVEC front panel, and through J1-31 to the CAC button of the CRO Switcher. A voltage divider consisting of R12 and R13 provides a bias of approximately −7.5 volts to the base of Q5. Bias voltage and dc feedback for the base of Q6 are obtained from Zener diode CR3 and resistor R17. AC feedback is provided by C3. R21 and C4 decouple the bias circuits from the −20 volt bus. Under zero input signal conditions, the collector of Q5 is at approximately −4 volts and the emitter of Q6 is at approximately −11 volts.

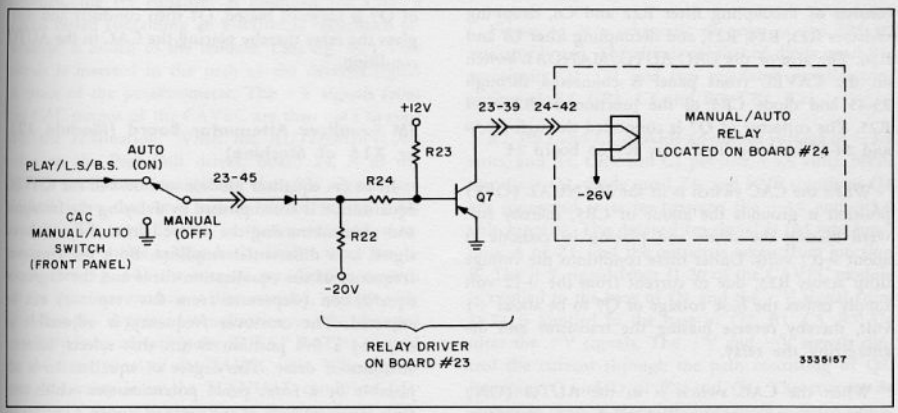
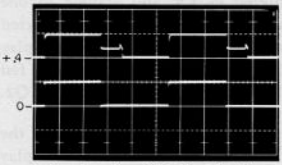
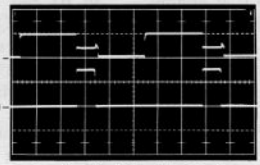


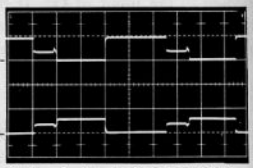
Figure 57—Simplified Diagram of AUTO/MANUAL Relay Circuit



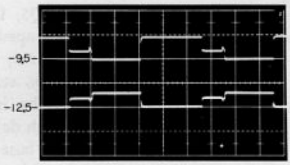
A. Top: Junction R10, C1, 0.5 v/cm
Bottom: 23-7 (WRITE PULSE), 2 v/cm
10 usec/cm



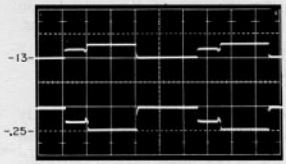
B. Top: Junction R10, C1, 0.5 v/cm
Bottom: 23-19 (CAC DISPLAY CLAMP), 2 v/cm
10 usec/cm



C. Top: Junction R13, R14 (Q5 IN), 0.5 v/cm
Bottom: Q5 Collector, 0.5 v/cm
10 usec/cm



D. Top: Q5 Emitter, 0.5 v/cm
Bottom: Q6 Base, 0.5 v/cm
10 usec/cm



E. Top: Q6 Emitter, 0.5 v/cm
Bottom: 23-25 (CAC CRO OUT), 0.5 v/cm
10 usec/cm

Figure 58—Waveforms, Board 23

Relay Driver

As shown in figure 131 the base bias of the relay driver, Q7 is determined by a network connected between the +12 volt and −20 volt supplies, which consists of decoupling filter R22 and C6, dropping resistors R23, R24, R25, and decoupling filter C7 and R26. The arm of the CAC AUTO/MANUAL switch on the CAVEC front panel is connected through 23-45 and diode CR5 to the junction of R24 and R25. The collector of Q7 is connected through 23-39 and 24-42 to the coil of relay K1 on board 24.

When the CAC switch is in the MANUAL (OFF) position it grounds the anode of CR5, thereby forward biasing the diode and placing its cathode at about −0.7 volts. Under these conditions the voltage drop across R23, due to current from the +12 volt supply causes the base voltage of Q7 to be about +1 volt, thereby reverse biasing the transistor and de-energizing the relay.

When the CAC switch is in the AUTO (ON) position, it connects the PLAY/L.S./B.S. bus from the logic circuit in the Burst Processor Module to CR5. When the machine is in the PLAY mode, and both the lock sense and burst sense conditions have been achieved this bus is at −20 volts, and CR5, therefore is reverse biased. The cathode of CR5 is then at about −4 volts, and the base-emitter junction of Q7 is forward biased. Q7 then conducts and energizes the relay thereby placing the CAC in the AUTO condition.

FM Equalizer Attenuator Board (Module 523, or X16 of Machine)

In an fm equalizer module unmodified for CAVEC equalization is accomplished by delaying the fm signal and then subtracting the delayed from the undelayed signal in a differential amplifier. Both the crossover frequency of the equalization curve and the degree of equalization (departure from flat response) can be adjusted. The crossover frequency is adjustable in steps by a five position switch that selects different amounts of delay. The degree of equalization is adjustable by a front panel potentiometer which controls the amplitude of the delayed signal. (The larger the signal in the delayed path the less the equaliza-

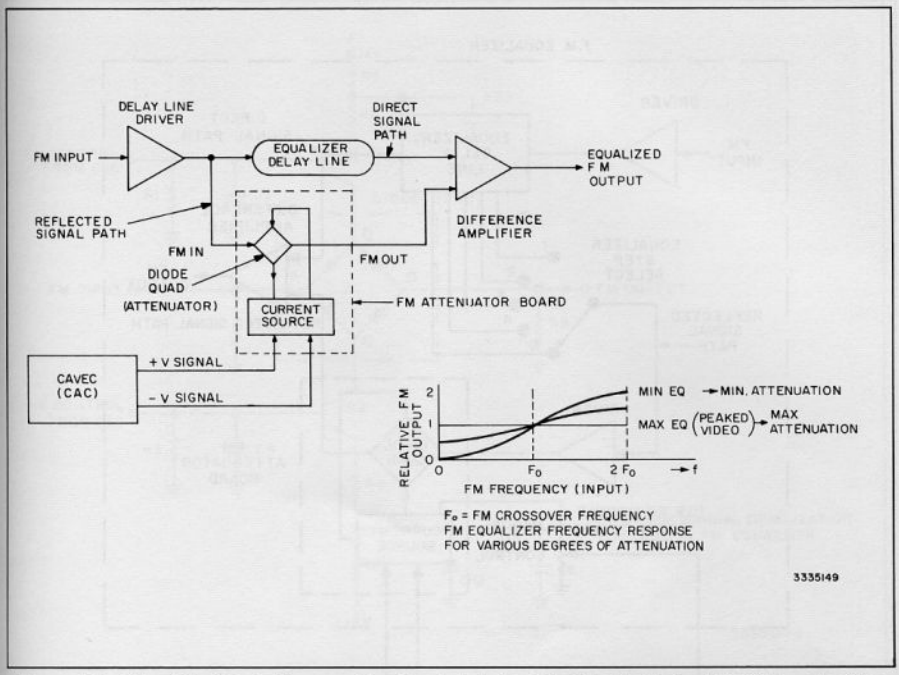


Figure 59—Simplified Block Diagram Showing Principle of Electrically Controlled FM Equalization

tion, and the smaller the chroma content of the video signal.)

When, the fm equalizer is modified for CAC a circuit board containing an electrically controlled attenuator is added to the module. (See fig. 59.) This circuit is inserted in the path of the delayed signal in place of the potentiometer. The ±V signals from the CAC output of the CAVEC are then used to control the attenuation. When the AUTO/MANUAL relay on the Push-Pull driver, board 24, is in the AUTO condition (energized) the ±V signals are derived from the error signals stored in the CAC memory. The equalization is thus controlled automatically on a line-by-line basis. Under these conditions, (see fig. 60) the manual equalization control on the equalizer module is disconnected, and the only way that the degree of equalization can be changed manually is by adjusting the BURST RATIO control on the front panel of the CAVEC unit. When, however, the relay is in the MANUAL condition (deenergized) the ±V signals are derived from a dc voltage which depends on the setting of the manual equalization potentiometer on the FM equalizer. The equalization can then be controlled manually by adjusting this potentiometer.

Figure 61 is a schematic diagram of the FM attenuator board. The circuit consists of diode quad Z1, transistors Q1, Q2, and two regulated supplies consisting of R4, CR1, C1 and R7, CR2, C2.

R7, CR2 and C2 provide an output voltage of −3.9 volts, and R4, CR1 and C1 provide +3.9 volts. NPN transistor Q2, diode quad Z1, and PNP transistor Q1 are connected in series between the −3.9 and +3.9 volt supplies. The delayed fm signal is fed into junction. A of Z1, and the output is taken from junction B. The +V signal from J1-20 of the CAVEC module is applied to the base of Q1 and the −V signal from J1-21 is applied to the base of Q2, R1, C3, R3, C4 filter the ±V signals. The +V and −V signals control the current through the path consisting of Q2, junctions C and D of Z1 and Q1. The current decreases as the +V signal assumes more positive values (and the −V signal assumes more negative values)

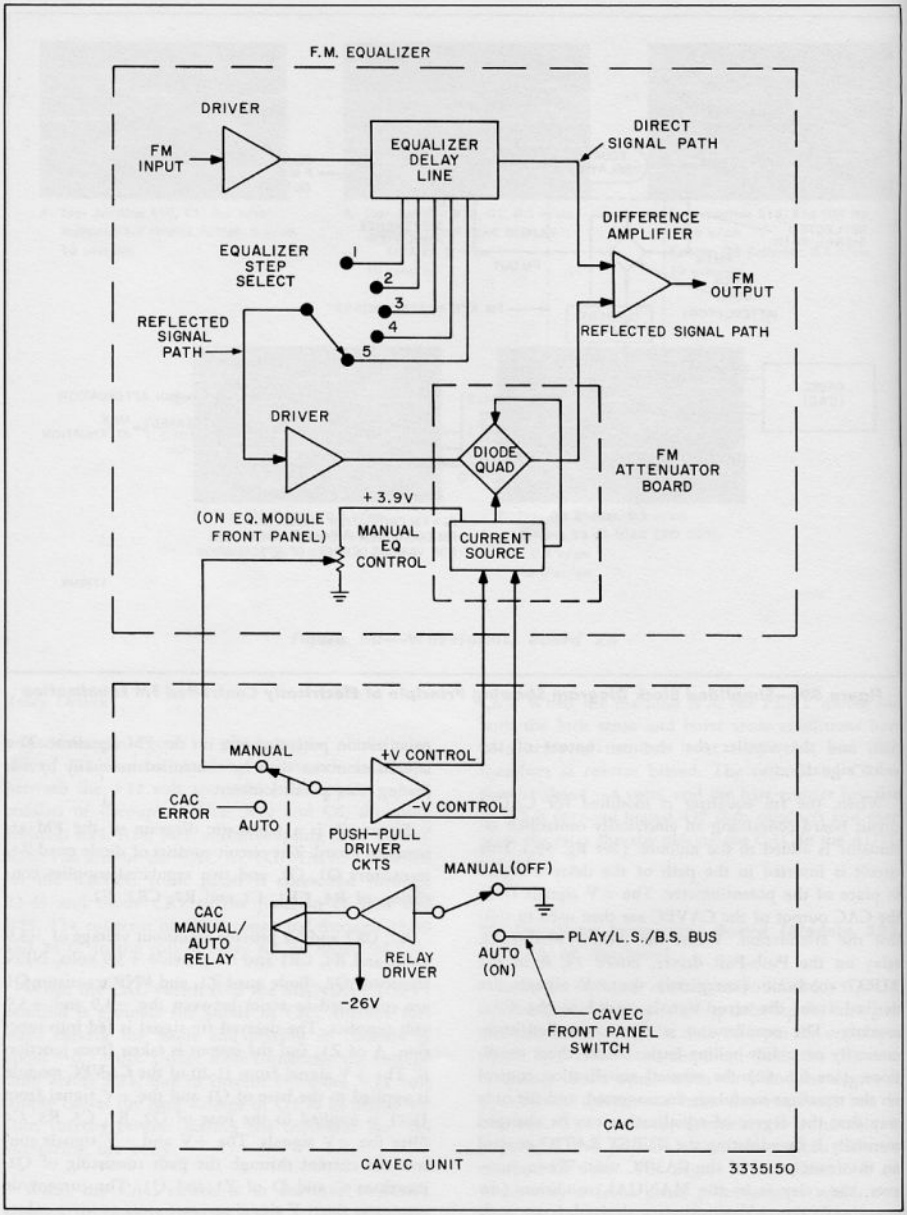


Figure 60—Partial Block Diagram Showing FM Equalization Control System

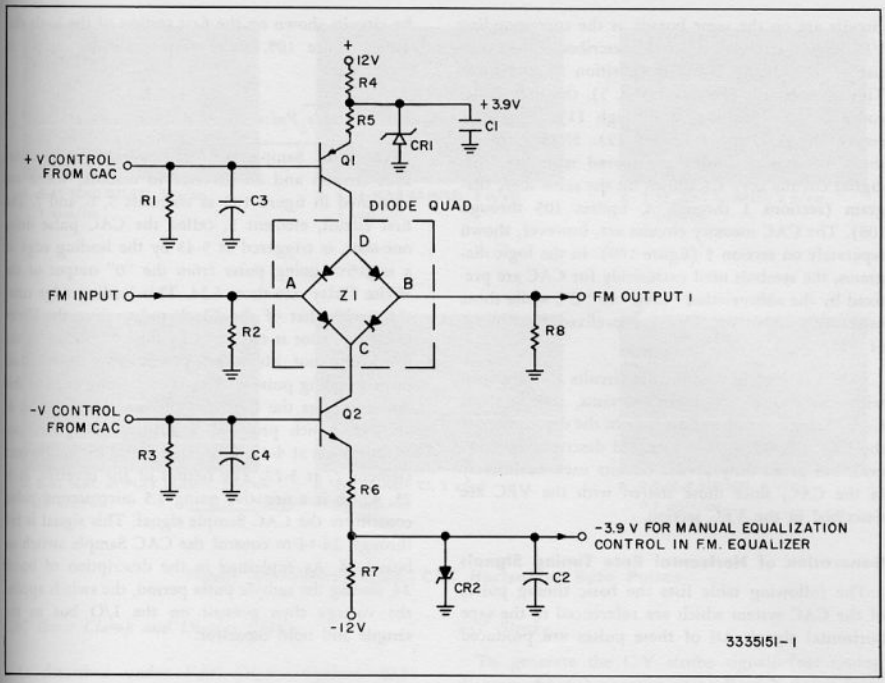


Figure 61—Simplified Schematic Diagram of FM Equalizer Attenuator Board

because the transistors approach cut off. For fixed values of +V and −V, however, the current is constant.

Since the four diodes are forward biased, the fm signal applied to junction A can flow through the quad to the output at junction B. The impedance between junctions A and B, however, depends on the amount of forward bias current. This, in turn, depends on the current supplied by Q1 and Q2. The quad, therefore, attenuates the fm input by an amount depending on the ±V signals. The larger the +V signal, the greater the delayed path FM signal attenuation and the greater the chroma content of the video. Conversely, the smaller the +V signal the less the attenuation and the smaller the chroma content of the video. Use of the two balanced push-pull drive signals reduces transient disturbances and distortion of the f-m signal.

The −3.9 volt Zener regulator circuit R7, CR2, and C2, in addition to providing bias to Q2, provides the input voltage to the manual equalization potentiometer on the f-m equalizer module. The arm of this potentiometer is connected through J1-6 of the CAVEC module, and 24-43 to a resistor divider connected to contacts K1-B of the AUTO/MANUAL relay, K1 (See section 7 of Logic Diagram). When the relay is de-energized, K1B feeds the attenuated potentiometer voltage to the input of the first push-pull driver stage. Consequently, since the ±V signals depend on the potentiometer voltage, the equalization can then be varied manually by adjusting the potentiometer. When, however, the relay is energized, K1B disconnects the potentiometer voltage and feeds the CAC error voltage from the sample and hold capacitor to the first push-pull driver. Under these conditions, the potentiometer has no effect, and the equalization is controlled automatically by the CAC signals from the capacitor memory.

DETAILED DESCRIPTION OF CAC DIGITAL SYSTEM

Except for the four CAC storage boards, which occupy positions 25 through 28, all of the CAC digital

circuits are on the same boards as the corresponding VEC digital circuits previously described. These consist of the Timing B board (position 2), the three Timing A boards (positions 3, 4, 5), the four X decoder boards (positions 8 through 11) and the Y switch driver board (position 12). Since many of the CAC digital circuits are shared with the VEC digital circuits they are shown on the same logic diagram (sections 1 through 4, figures 105 through 108). The CAC memory circuits are, however, shown separately on section 5 (figure 109). In the logic diagrams, the symbols used exclusively for CAC are prefixed by the abbreviation "CAC" or "C", while those used exclusively for VEC are prefixed by "VEC" or "V".

In the following sections the circuits are described with reference to the logic diagrams, starting with CAVEC logic detail section 1, as in the description of the *VEC Digital System*. Detailed descriptions, however, are given only of the circuits used exclusively in the CAC, since those shared with the VEC are described in the VEC section.

Generation of Horizontal Rate Timing Signals

The following table lists the basic timing pulses of the CAC system which are referenced to the tape horizontal signal. All of these pulses are produced by circuits shown on the first section of the logic diagram, figure 105. Pulse waveforms are shown in figure 62.

$\overline{\text{CAC Sample}}$ Pulse

The $\overline{\text{CAC Sample}}$ pulse is produced by two one-shot circuits and an inverter in cascade, which are identified in figure 105 as elements 5, 6, and 7. The first circuit, element 5, called the CAC pulse delay one-shot, is triggered at 5-43 by the leading edge of a negative going pulse from the "0" output of the Write Delay one-shot, 4-34. This leading edge coincides with that of the Clock pulse, since the Write delay one shot is triggered by the "0" output of the Clock one-shot. Element 5, produces a 1 microsecond positive going pulse at 5-41. The trailing edge of this pulse triggers the CAC Sample one-shot, element 6, at 4-43, which produces a positive going 1.5 μsec output pulse at 4-41. This pulse is fed to the inverter, element 7, at 5-27. The output of the inverter, at 5-25, which is a negative going 1.5 microsecond pulse, constitutes the $\overline{\text{CAC Sample}}$ signal. This signal is fed through 24-14 to control the CAC Sample switch on board 24. As explained in the description of board 24, during the sample pulse period, the switch applies the voltage then present on the I/O bus to the sample and hold capacitor.

BASIC HORIZONTAL RATE TIMING PULSES

Pulse Name	*Function*	*Delay of Pulse Leading Edge with Respect to Tape Horizontal Leading Edge (usec)*	*Pulse Width (usec)*
Clock*	Provides basic horizontal rate timing reference	0	0.5
Read X*	Determines read time of capacitor memory	0.5	4.3
$\overline{\text{CAC Sample}}$	Closes CAC sample switch on board 24	1	1.5
Write*	Closes CAC Write switches on boards 23 and 29	8.5	32
Write X*	Determines Write time of capacitor memory	26.5	15
CAC Burst Clamp	Closes Clamp switch on board 29 to discharge capacitor of threshold detector	40.5	10
CAC Display Clamp	Closes Display Clamp switch on board 23	40.5	10
C-Y Strobe	Determines time during which Y switches of CAC capacitor memory are closed	**	

* These pulses are shared with the VEC and are generated as described under *VEC Digital System.*

** C-Y Strobe signal is generated by OR gating Read X and Write X pulse, and therefore goes high during both pulse periods

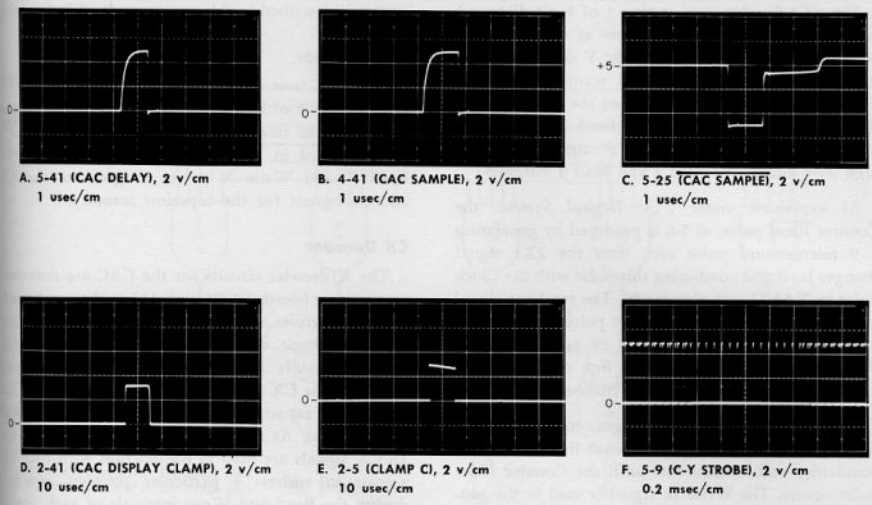


Figure 62—Waveforms, CAC Horizontal Rate Pulses

CAC Burst Clamp and Display Clamp

As described under *VEC Digital System,* 40.5 microseconds after the leading edge of the Clock pulse, the Clamp one-shot (element 43 in figure 105) produces a negative going 10 microsecond pulse at its "0" output, 2-43, and a positive going 10 microsecond pulse at its "1" output, 2-41. The positive going output, which constitutes the CAC Display Clamp pulse, is fed through 23-19 to the display clamp switch. As explained in the circuit description of board 23, the switch closes during the clamp pulse period and applies the attenuated +V signal to the CRO driver amplifier.

The negative going output pulse of the Clamp one shot is fed through 2-4 to an inverter. The inverter output, at 2-5 constitutes the CAC Burst Clamp pulse. This pulse is fed through 29-1 to the Burst Clamp switch. During the clamp pulse period, the switch closes and discharges the output capacitor (C5) of the threshold detector, thereby allowing it to charge to a new voltage during the next line.

Note that both of the CAC clamp pulses are identical to the VEC Clamp Drive pulse, except that these pulses occur in every line while the VEC Clamp Drive pulse is inhibited during line 1.

C-Y Strobe

To generate the C-Y strobe signal, (see timing diagram, fig. 63) negative going Read X pulses from the "0" output of the Read one shot, 2-34 are fed to one input of an OR gate at 5-10 and negative going Write X pulses from 4-14 are fed to the other input of the gate at 5-11. The gate output at 5-9, therefore, which constitutes the C-Y strobe, is normally low, but goes high during both the Read X and Write X period of each line. (As explained under *VEC Digital System,* the Write X pulse is inhibited for 830 microseconds during the vertical interval. During this period, therefore, the gate output contains only Read X pulse). The C-Y strobe is fed through 12-7 to the Y decoder circuits, where it is combined with the 2X1 and 4X2 signals to produce the CY memory address signals.

Basic Timing Signals Derived From 4X2 and 2X1 Switcher Signals

The CAC system uses the same signals based on the 4X2 and 2X1 switcher signals as the VEC System. These signals consist of the following:

a. 4X2 Flip-Flop signals.

b. Counter $\overline{\text{Reset}}$ pulse.

c. $\overline{\text{Write 16}}$ pulse.

The 4X2 flip-flop (see section 1 of logic diagram) produces two output signals, one at 6-15, and the other at 6-13 which are used in the Y decoder circuits to permit identifying the head scanning intervals. The signal at 6-13, which is called the 4X2 F.F. "0" signal is high only during the head 1 and head 2 intervals, while the 4X2 F.F. "1" signal at 6-15 is high only during the head 3 and head 4 intervals.

As explained under *VEC Digital System,* the Counter $\overline{\text{Reset}}$ pulse, at 5-6 is produced by generating a 9 microsecond pulse each time the 2X1 signal changes level and combining this pulse with the Clock pulse in NAND gate element 29. The resulting signal is a negative going, counter reset pulse which occurs only at the beginning of line 1 of each head scan. This pulse is used to reset the line counter to the condition corresponding to line number 1.

The $\overline{\text{Write}}$ 16 signal at 7-22 goes low only at the start of a seventeenth line (sixteenth line on 625 line standards) and remains low until the Counter Reset pulse occurs. The Write 16 signal is used in the generation of the CX16 signal, to cause the sixteenth capacitor in each section of the memory bank to be written into only during the sixteenth line (or fifteenth line on 625 line standards). Generation of the Write 16 signal is described in the section on the VEC Digital System. Use of this pulse in the CAC system is described in this section under *CX Decoder.*

Line Counter

The CAC uses the same line counter as the VEC (see section 2 of Logic Diagram). The eight output signals of the counter (2^0, $\overline{2^0}$, 2^1, $\overline{2^1}$, 2^2, $\overline{2^2}$, 2^3, $\overline{2^3}$) are combined in the CX decoder circuits with the Read X and Write X pulses to generate the CX address signals for the capacitor memory.

CX Decoder

The X decoder circuits for the CAC are contained on the same boards (8 through 11) as the corresponding VEC circuits and are shown in sections 2, 3, and 4, of the logic diagram. The purpose of the CX decoder circuits is to produce 16 unique signals known as the CX Address signals, one for each of the 16 memory capacitors corresponding to a given head scan interval. As explained under *CAC Memory* the 16 CX signals are used in conjunction with four CY signals to address a particular memory capacitor during the Read and Write intervals of each line.

The sixteen CX signals are designated CX1 through CX16. Each of these signals corresponds to a given scanning line number in a head interval, and goes high during the Read X and Write X period of that line (except for CX16, as described later).

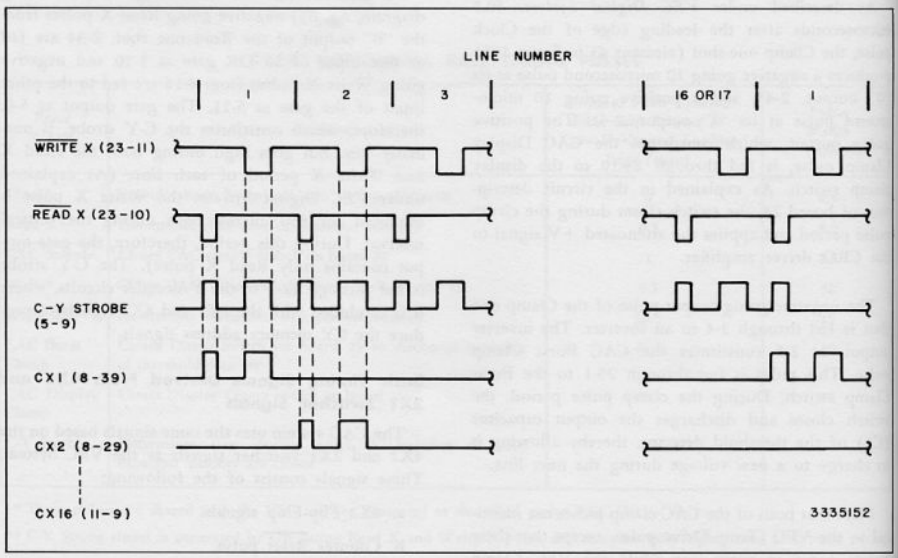


Figure 63—Generation of C-Y Strobe

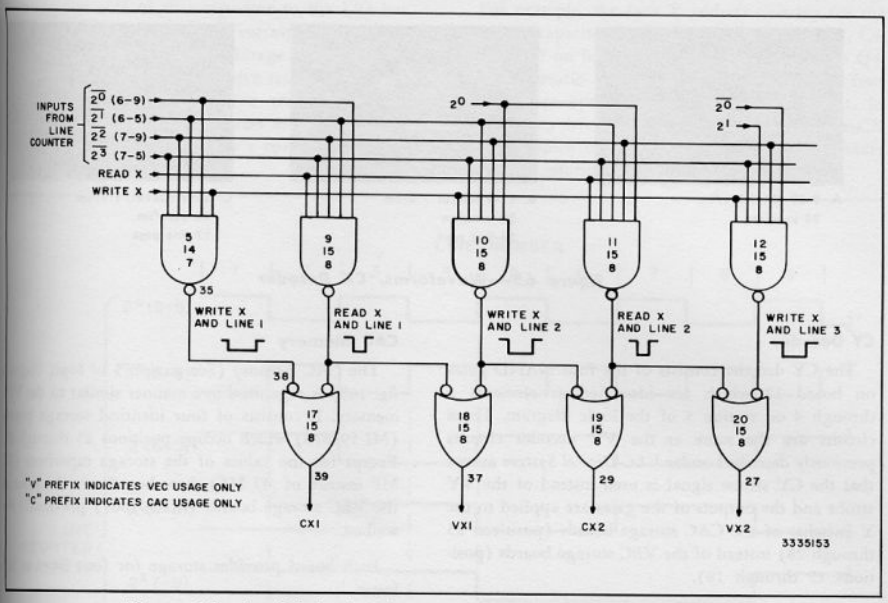


Figure 64—Partial Logic Diagram Showing CX Decoder Circuits

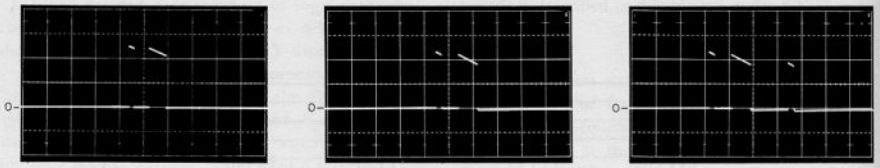
NOTE: On 625 line standards, only 15 CX signals (CX2 through CX16) are generated because each head scanning period contains one line less than on 525 line standards.

Each CX signal is generated by using two NAND gates and an OR gate as shown in figure 64. The two NAND gates for CX1 are identified in figure 64 as elements 5 and 9, and the OR gate as element 17.

The particular four outputs of the counter that go high during line 1 of each head scan (525 line operation only) are fed to both NAND gates. In addition, the Write X pulse is fed to the first NAND gate and the Read X pulse to the second NAND gate. The output of the NAND gate (element 5), therefore goes low during the Write X period of line 1 and the output of the second NAND gate (element 9) goes low during the Read X period of line 1. The outputs of elements 5 and 9 are each fed to one input of the OR gate, element 17. The output of this gate, therefore, which constitutes the CX1 signal, goes high during both the Read X and Write X periods of line 1. (See Timing Diagram, figure 66.)

The other CX signals (except for CX16) are generated in the same manner. Note that the same NAND gates are used for decoding the VX signals. Different OR gates, however, are used because each VX signal goes high during the Read and Write periods of succeeding lines instead of the same line.

The decoding circuit for CX16 is modified slightly to prevent writing into the sixteenth capacitor again during the seventeenth line (sixteenth line of 625 line standards). Generation of the CX16 signal is accomplished by two NAND gates, elements 6 and 7, and an OR gate, element 15, as shown in section 4 of the logic diagram. The only difference between this circuit and the others is that element 6 has six inputs instead of five, and the Write 16 signal from 7-22 is applied to the additional input. The Write 16 signal goes low only during the seventeenth line (sixteenth line on 625 line standards) when one occurs. Therefore, in the sixteenth line (of either a 16 or 17 line scan), the CX16 signal goes high during both the Read X and Write X period. (See waveforms, figure 65B, 65C). During a seventeenth line, the line counter remains in the line 16 condition. The output of NAND gate element 7, therefore goes low during the Read X interval, but the output of element 6 which normally would go low during the Write X interval remains high, because the Write 16 input to that gate is low. The CX16 signal, therefore goes high only during the Read X interval of line 17.



A. 8-39 (CX1) 1 v/cm
20 usec/cm

B. 11-9 (CX16) 1 v/cm
20 usec/cm
16-line pass

C. 11-9 (CX16), 1 v/cm
20 usec/cm
17-line pass

Figure 65—Waveforms, CX Decoder

CY Decoder

The CY decoder consists of the four NAND gates on board 12 which are identified as elements 1 through 4 on section 5 of the logic diagram. These circuits are the same as the VY decoder circuits previously described under *VEC Digital System* except that the CY strobe signal is used instead of the VY strobe and the outputs of the gates are applied to the Y switches of the CAC storage boards (positions 25 through 28) instead of the VEC storage boards (positions 15 through 18).

As in the VY decoder, each gate corresponds to one of the four head scanning intervals. The inputs to each gate consist of the CY strobe and two signals which go high simultaneously only during the head scan corresponding to the gate as shown in the following table:

INPUTS TO CY DECODER

Signals Simultaneously High	*Head Scan Interval*	*Element Number to which Signal is applied (See Section 5 of Logic Diagram)*
2 X 1 and 4 X 2 F.F. "0"	1	1
$\overline{2\ X\ 1}$ and 4 X 2 F.F. "0"	2	2
2 X 1 and 4 X 2 F.F. "1"	3	3
$\overline{2\ X\ 1}$ and 4 X 2 F.F. "1"	4	4

As previously mentioned, the CY strobe goes high during the Read X and Write X periods of every line (including the seventeenth, when one is present). Consequently the output of each gate goes low only during the Read X and Write X intervals of each line in the corresponding head scan period. The gate outputs constitute the CAC memory Y address signals $\overline{CY1}$ through $\overline{CY4}$.

CAC Memory

The CAC memory (See section 5 of logic diagram fig. 109) is organized in a manner similar to the VEC memory. It consists of four identical storage boards (MI-591618) which occupy positions 25 through 28. Except for the values of the storage capacitors (2.2 MF instead of .47 MF) these boards are the same as the VEC storage boards (MI-591607) previously described.

Each board provides storage for four lines as follows:

Board 28—Lines 1 through 4

Board 27—Lines 5 through 8

Board 26—Lines 9 through 12

Board 25—Lines 13 through 16

As in the VEC memory, the sixteen capacitors on each board comprise four groups, one for each of the four lines. Each of these groups, in turn, contains one capacitor for each of the four head scans. For example, on board 28, the group consisting of C1, C4, C5, C7 provides storage for line 1. In the order given, these capacitors correspond to head scans 1 through 4. Similarly the capacitors in corresponding locations on the board in position 27, and having the same schematic symbol numbers provide storage for line 5, and head scans 1 through 4.

> NOTE: Since there are four identical storage boards, each component shown or the schematic can have any of four functions depending on the position occupied by the board. See the table headed *Functions of Components on Digital and Memory Boards* for details.

Each board contains sixteen X address switches, Q1 through Q16 and one Y address switch, Q17. Each X address switch corresponds to one of the 16 capacitors on the same board, and when energized it

connects one side of that capacitor to the I/O bus. The four X address switches corresponding to the group of capacitors providing storage for a given line are operated from the same drive transformer. Consequently there are four drive transformers, T1 through T4, for the 16 X address switches. Each of these transformers is driven by a corresponding CX address signal.

For example, the four X address switches for the group of capacitors corresponding to line 1 (C1, C4, C5 and C7 on board 28) consist of Q1 through Q4. (See schematic diagram figure 155.) These four switches are operated by drive transformer T1. In turn, T1, is driven by the CX1 signal from the CX decoder which is fed through 28-41 to the primary of the transformer.

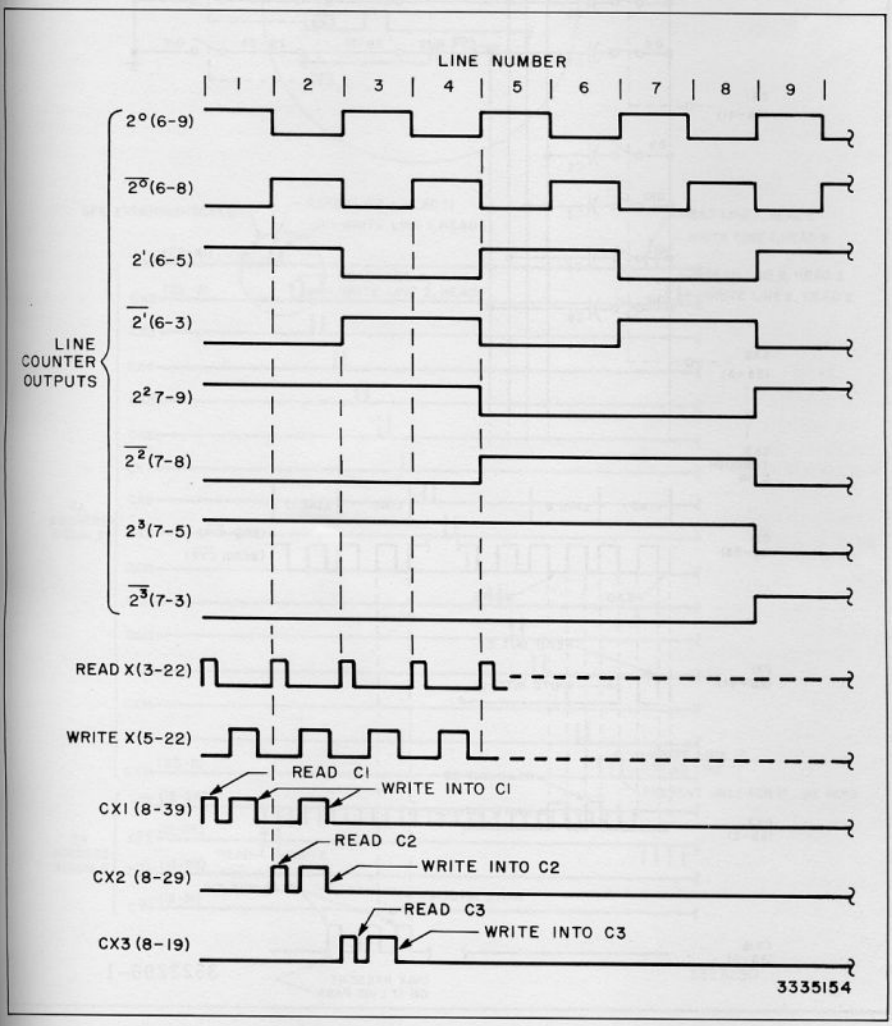


Figure 66—Timing Diagram Showing Generation of CX Memory Address Signals

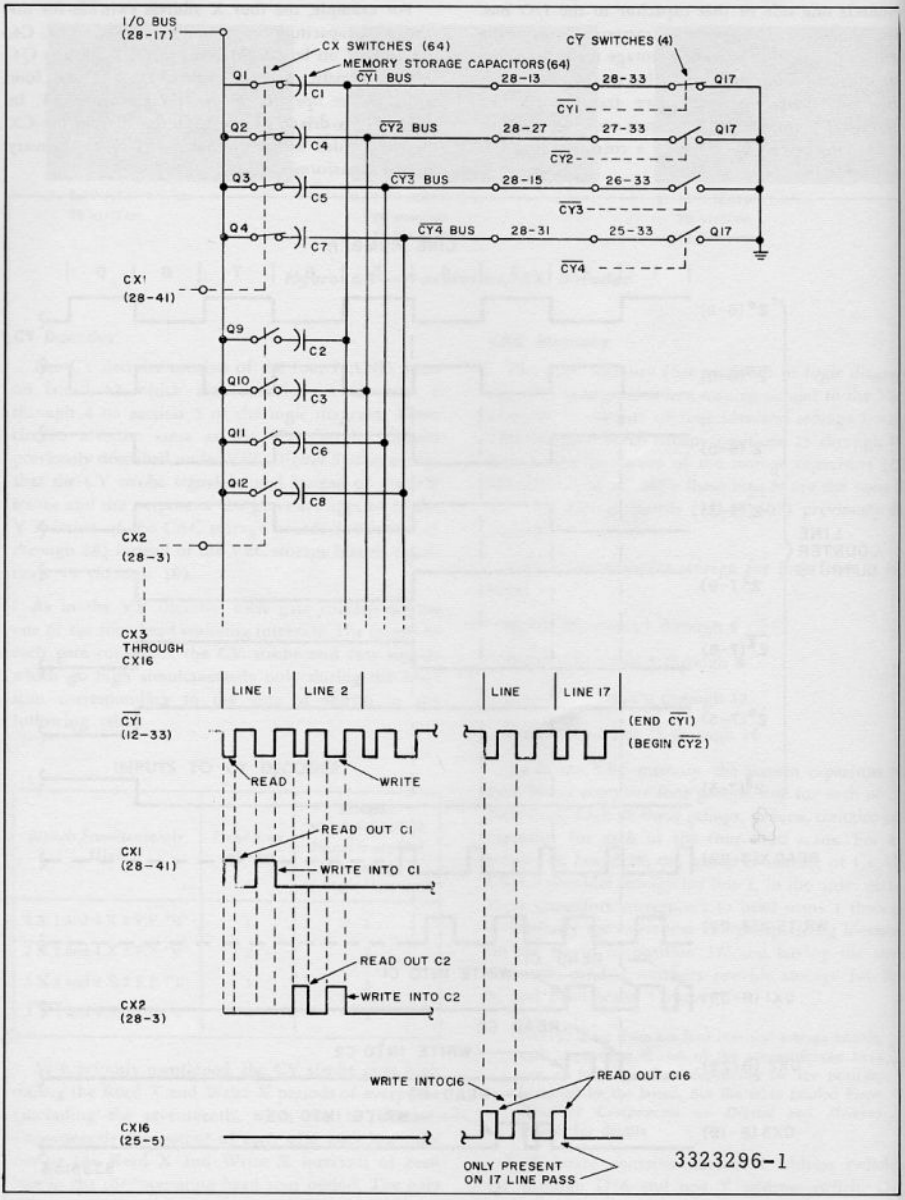


Figure 67—Simplified Diagram of CAC Memory Address Matrix

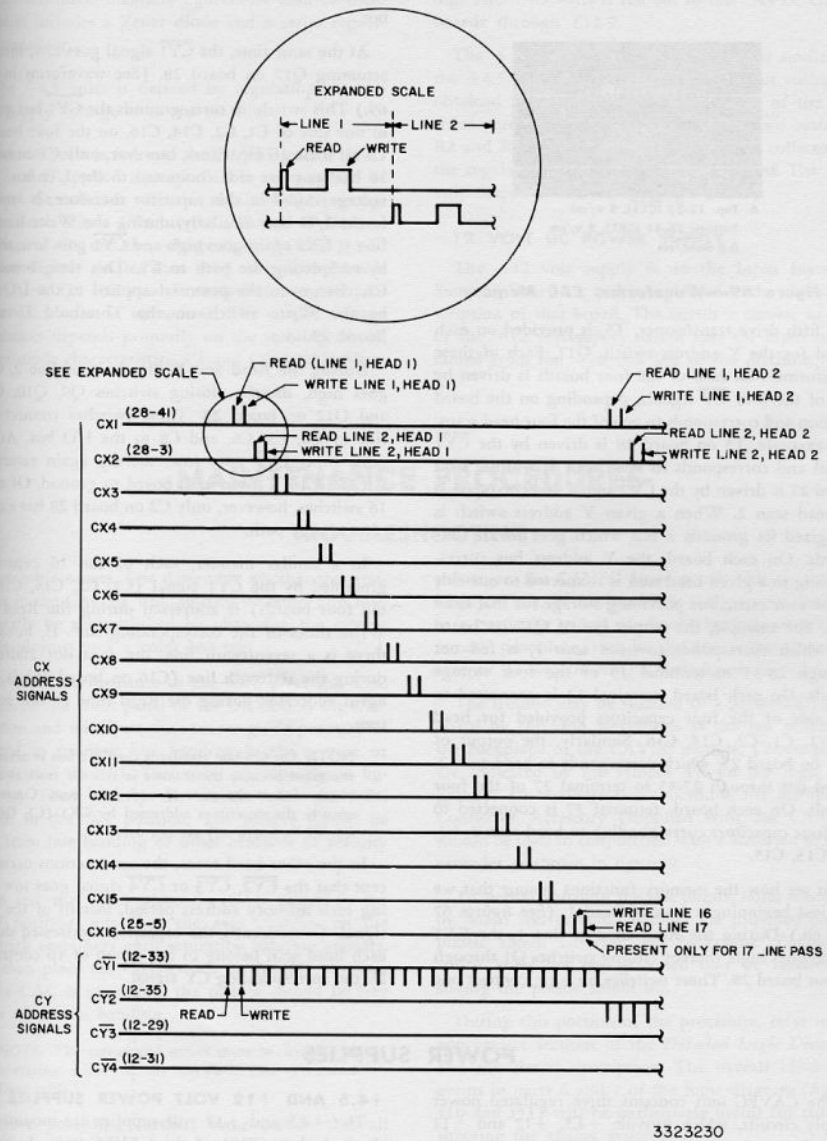
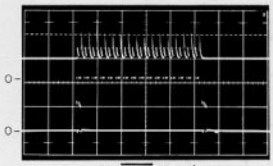


Figure 68—Timing Diagram Showing CAC Memory Addressing



A. Top: 12-23 $\overline{CY1}$), 5 v/cm
Bottom: 28-41 (CX1), 2 v/cm
0.2 msec/cm

Figure 69—Waveforms, CAC Memory

A fifth drive transformer, T5, is provided on each board for the Y address switch, Q17. Each of these transformers on each of the four boards is driven by one of the four $\overline{CY}$ signals, depending on the board position and corresponds to one of the four head scans. For example, T5 on board 28 is driven by the $\overline{CY1}$ signal and corresponds to head scan 1, while T5 on board 27 is driven by the $\overline{CY2}$ signal and corresponds to head scan 2. When a given Y address switch is energized its grounds a bus which goes to all four boards. On each board, the Y address bus corresponding to a given head scan is connected to one side of the four capacitors providing storage for that head scan. For example, the output bus of Q17 on board 28, which corresponds to head scan 1, is fed out through 28-33 to terminal 13 of the four storage boards. On each board, terminal 13 is connected to one side of the four capacitors provided for head scan 1, C1, C2, C14, C16. Similarly, the output of Q17 on board 27, which corresponds to head scan 2, is fed out through 27-33 to terminal 27 of the four boards. On each board, terminal 27 is connected to the four capacitors corresponding to head scan 2, C3, C4, C13, C15.

To see how the memory functions assume that we are just beginning a scan of head 1. (See figures 67 and 68.) During the Read time of line 1, the CX1 signal goes high, thereby closing switches Q1 through Q4 on board 28. These switches, in turn, connect one side of C1, C4, C5, and C7 on board 28 to the I/O bus.

At the same time, the $\overline{CY1}$ signal goes low, thereby actuating Q17 on board 28. (See waveforms in fig. 69.) This switch, in turn, grounds the $\overline{CY1}$ bus going to one side of C1, C2, C14, C16, on the four boards. Of all these 16 capacitors, however, only C1 on board 28 has its other side connected to the I/O bus. The voltage stored in this capacitor therefore, is applied to the I/O bus. Similarly, during the Write time of line 1, CX1 again goes high and $\overline{CY1}$ goes low, thereby completing the path to C1. This time, however, C1, charges to the potential applied to the I/O bus by the Write switch on the Threshold Detector Board 29.

During the Read and Write times of line 2, CX2 goes high, thereby closing switches Q9, Q10, Q11, and Q12 on board 28. These switches connect one side of C2, C3, C6, and C8 to the I/O bus. At the same time, $\overline{CY2}$ goes low, thereby again returning C1, C2, C14, C16 on each board to ground. Of these 16 switches, however, only C2 on board 28 has a complete charge path.

In a similar manner, each of the 16 capacitors grounded by the $\overline{CY1}$ signal (C1, C2, C14, C16 on the four boards) is addressed during the Read and Write times of the corresponding line. If, however, there is a seventeenth line, the capacitor addressed during the sixteenth line (C16 on board 25) is once again addressed during the Read time of line seventeen.

> NOTE: On 625-line standards the CX1 bus is never energized because the counter is actually reset to a count of 2 at the start of each head scan. Consequently the capacitors addressed by CX1 (C1, C4, C5, C7 on board 28) are not used.

In the other head scans, the same actions occur except that the $\overline{CY2}$, $\overline{CY3}$ or $\overline{CY4}$ signal goes low during each memory address period, instant of the $\overline{CY1}$ signal. Consequently the capacitors addressed during each head scan belong to the group of 16 controlled by the corresponding $\overline{CY}$ signal.

POWER SUPPLIES

The CAVEC unit contains three regulated power supply circuits, which provide +4.5, +12 and −12 volts dc.

+4.5 AND +12 VOLT POWER SUPPLIES

The +4.5 and +12 volt supplies are mounted on the end plate (E12) of the CAVEC unit. As shown

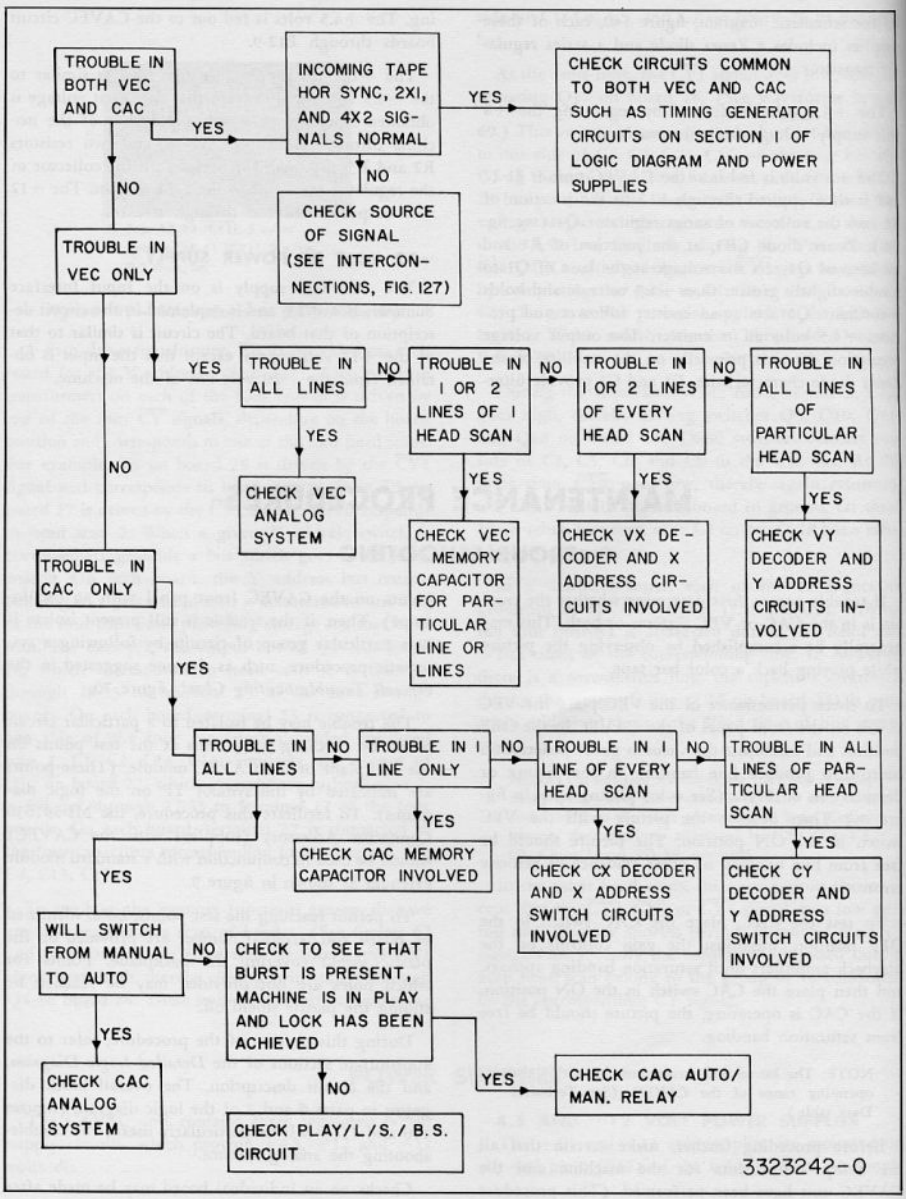


Figure 70—Overall Trouble Shooting Chart

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